ANALYSIS AND COMPARISON OF LEAKAGE POWER REDUCTION TECHNIQUES FOR VLSI DESIGN

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***Abstract*—**Gadgets consuming less power have risen as a well-known subject in the cutting-edge electronics industry. Decrease in consumption of power makes a device increasingly dependable and productive. As a result, CMOS innovation turned out to be most popular for low power utilization gadgets. Cutback on the voltage supply decreases the dynamic power loss quadratically and the leakage power linearly. Weak inversion current due to leakage is a prime candidate for standing power utilization. Since the feature sizes continue to reduce it has caused an exponential rise in weak inversion current due to leakage thanks to the reduction of sub-threshold voltage. As stated in the previous works, leakage power dissipation sooner or later may tower above the total power consumption as the size of technological features reduce to nano-meter scheme in submicron technologies. This paper is aimed to bring a thorough analysis and comparison of various leakage power reduction techniques used.

Keywords: Leakage current sub-threshold voltage, deep submicron, power gating, CMOS, LECTOR, power dissipation

I. INTRODUCTION

The rapid increase in semiconductor technology led the feature sizes to be shrinking by using deep-submicron processes. System on a chip (SoC) is an integrated circuit that integrates complex functions on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements.

With miniaturization and the growing trend towards wireless communication, power dissipation has become a very critical design metric. The longer the battery lasts, the better is the device. With the advancement in technology, static power dominates dynamic power. Leakage currents are especially important in burst mode type integrated circuits where most of the time the system is in an idle, or sleep mode. No computation takes place during sleep mode [1]. For example, a cell phone will be in the standby mode for most of the time where the processor is in idle state. With the large leakage currents during the idle mode power will be continuously drained with no useful work being done. Many techniques have been proposed [2] to minimize these leakage currents in nanometer technology. Excessive power dissipation in portable devices causes overheating, reduces chip life, functionality and degrades performance. Minimizing power consumption is therefore important and necessary, both for increasing levels of integration and to improve reliability, feasibility and cost.

II. RELATED WORK

Leakage power dissipation is the dominant contributor of total power dissipation in nanoscale complementary metal oxide semiconductor (CMOS) integrated circuits. CMOS technology scaling demands for a reduced power supply, low threshold voltage, high transistor density and reduced oxide thickness, which has led to significant increase in leakage power especially during standby mode. Here in this paper, at first we review some of the existing techniques for leakage minimization and pointed out their merits and shortcomings. We then propose a novel transistor level approach called leakage control NMOS transistor (LCNT) for leakage minimization. The proposed technique inserts two leakage control transistors (all N-type) within a standard CMOS logic circuit. The gate terminal of the leakage control transistors are connected with the drain of the pull-up transistors. Performance of the proposed technique is investigated in terms of area, power, delay, and power-delay product applying on some basic gates and benchmark circuits. The performance metrics of the proposed LCNT are

then compared with other existing techniques. Extensive SPICE simulations were carried out using 32 nm predictive technology model. Simulation results indicate that the proposed technique is quite efficient in minimizing the leakage power which is found out to be 48.4 %.

Device scaling is an important part of the very large scale integration (VLSI) design to boost up the success path of VLSI industry, which results in denser and faster integration of the devices. As technology node moves towards the very deep submicron region, leakage current and circuit reliability become the key issues. Both are increasing with the new technology generation and affecting the performance of the overall logic circuit. The VLSI designers must keep the balance in power dissipation and the circuit's performance with scaling of the devices. In this paper, different scaling methods are studied first. These scaling methods are used to identify the effects of those scaling methods on the power dissipation and propagation delay of the CMOS buffer circuit. For mitigating the power dissipation in scaled devices, we have proposed a reliable leakage reduction low power transmission gate (LPTG) approach and tested it on complementary metal oxide semiconductor (CMOS) buffer circuit. All simulation results are taken on HSPICE tool with Berkeley predictive technology model (BPTM) BSIM4 bulk CMOS files. The LPTG CMOS buffer reduces 95.16% power dissipation with 84.20% improvement in figure of merit at 32 nm technology node. Various process, voltage and temperature variations are analyzed for proving the robustness of the proposed approach. Leakage current uncertainty decreases from 0.91 to 0.43 in the CMOS buffer circuit that causes large circuit reliability.

III. EXISTING SYSTEM

In this technique or method, two transistors i.e. LCTs(leakage control transistors) are inserted between pull-up network (PUN) and pull-down network(PDN) within the logic block(a PMOS for pull-up network and an NMOS for pull down network) for which the gate terminal of each

LCT(leakage control transistor) is controlled by the source of the other transistors. The effective stacking of transistors in the path from the supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. Figure 1 shows the diagram of LECTOR technique.

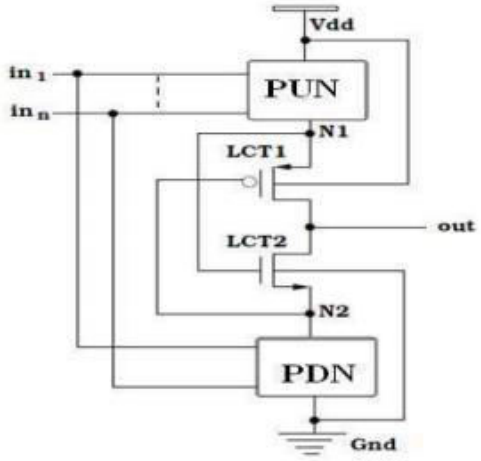

Fig. 1 Diagram of LECTOR technique

The elemental thought in this technique is leakage power reduction by embedding extra OFF transistors between the pull-up and pull-down networks. In our work, we applied this technique to the number of CMOS logic circuits and found that this reduction technique reduces the power dissipation as compared to traditional (conventional) and in the result, the table shows that the LECTOR technique yields better than conventional circuit.

IV. PROPOSED SYSTEM

This proposed technique is the basic circuit that approaches for reducing the leakage current in CMOS logic circuits. This technique is called stack ONFIC because for any output our logic block must be in 'ON' and 'OFF' condition.

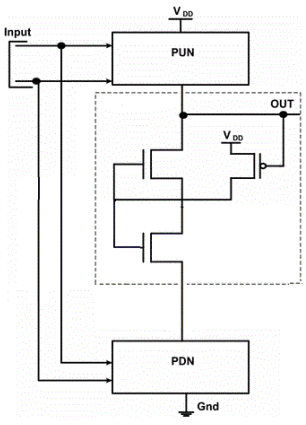

Fig. 2 Diagram of proposed technique

The proposed reduction technique contains a logic block which inserted between the pull-up and pull-down networks. In this technique, the logic block contains two leakage control transistors (LCTs) NMOS. Extra inserted PMOS drain terminal is connected to the gate terminals of two NMOS and gate terminal of PMOS is connected to the output. This technique gives the most hindrance to the stack ONOFIC block when it is in OFF state and least hindrance when it is in ON case[14]. This logic block directly affects the power dissipation and propagation delay of the logic circuit. In this work, we have proposed XOR, XNOR with the help of NAND gate.

This technique is further illustrated with the help CMOS inverter gate as shown in following figures.

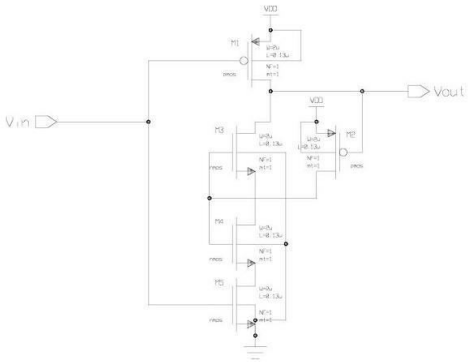

Fig. 3 CMOS inverter with stack ONOFIC

Table 1. Transistor Operation of stack ONOFIC CMOS Inverter

Input logic	PMOS	Stack ONOFIC PMOS	Stack ONOFIC NMOS (both)	NMOS
0	ON	OFF	OFF	OFF
1	OFF	ON	ON	ON

As table 1 shows that, when 0 logic is given as input then PMOS in PUN is ON and NMOS in PDN is OFF and Vdd supply voltage (1V) to drain terminal and passes to output, which is connected to gate of ONOFIC PMOS and turns OFF the PMOS (ONOFIC) which results in no voltage for both NMOS (ONOFIC) and turns OFF both ONOFIC NMOS. Similarly, in case of 1 logic, the PMOS in PUN is OFF. In figure 3, the CMOS inverter is simulated at 130nm and 22nmtechnology nodes with stack ONOFIC technique in which we get the following results as shown in table 2.Table 2 shows the simulated result of CMOS Inverter with proposed technique.

Table 2. simulated result of CMOS Inverter with proposed technique.

Parameters	130nm	22nm
Power dissipation (nW)	0.6687	2.6510
Delay (ps)	57.388	9.888

V. RESULTS

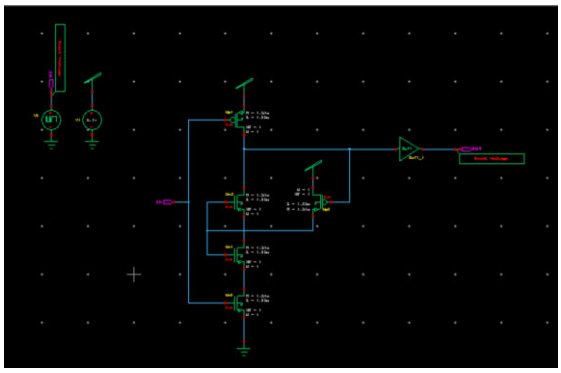

Fig - 4: Proposed onofic Inverter

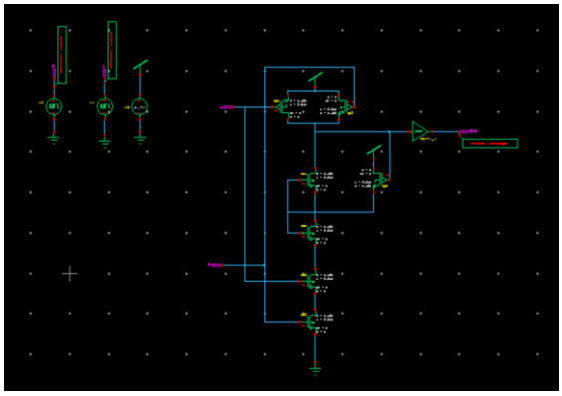

Fig - 5: Proposed Onofic Nand Gate

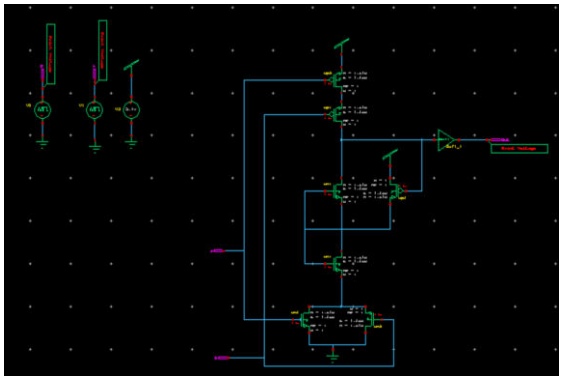

Fig - 6: Proposed Onofic NOR Gate

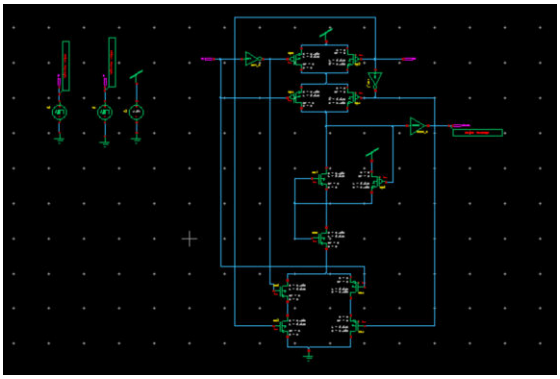

Fig - 7: Proposed Onofic Xor Gate

Ideal input = constnt input ==leakage power

input are chnages that circuit is active not ideal = active = power consumption

leakage power 8.470329e-022 watts = 8470 xe pow -18 (onofic)

leakage power -> 41.68990e-022 watts (Cmos Convention)

Average power consumed -> 4.154258e-008 watts (more leakage)

Average power consumed -> 7.424773e-021 watts

Average power consumed -> 8.311511e-021 watts

VI. CONCLUSION

In CMOS circuits, leakage power has become a more dominating component of total power consumption in battery oriented applications. Our proposed stack ONOFIC method gives low power dissipation when compared to other circuits. Here in this paper, the problem of power dissipation is reduced for different VLSI CMOS circuits. We simulated all circuits by using Tanner. It is helpful in saving power by reducing leakage power(power dissipation).Hence, ours proposed stack ONOFIC technique produces good results for reducing power dissipation as compared to other techniques.

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