JES
Journal of Engineering Sciences

Vol 13, Issue 01, Jan /2022
ISSN NO:0377-9254

Power Reduction in Domino Logic using clock gating in 16nm CMOS Technology

Soorampudi Mahalakshmi,
M.Tech,Roll Number-14A91D7218,
Aditya Engineering College, Surampalem

Baddireddy Satya Sridevi,
Associate Professor.
Aditya Engineering College,

ABSTRACT

A cmos domino thinking system uses clock gating in essentially a similar way as result hold circuitery. Clock is passed to the domino thinking simply during the intriguing state of the circuit. During hold mode, clock is avoided while the state of the circuit is held. A 2:1 multiplexer is used for clock gating and for holding the state of the circuit. Domino Logic has wound up being a basic circuit in VLSI improvement. Domino thinking likes obvious advantage like little district and quick advancement when appeared differently as per its static cmos . Domino Logic has wound up being a useful circuit in VLSI headway. Domino thinking likes grouped advantage like little locale and high speed advancement when appeared contrastingly practically identical to its static cmos entrance. The power of the proposed circuit is lessened to a typical of 99.37 percent concerning standard domino thinking

1. INTRODUCTION

To achieve better execution of the cmos device circuit close by high densities, there have been reduces in supply voltages, contraption focuses and semiconductor edge voltages all through the significant length. Regardless, these declines have correspondingly achieved higher spillage streams that can truly influence power usage in a circuit. The power comsumption of any cmos VLSI circuit is delivered utilizing stunning power and static power. The earth shattering power spread is a result of the trading activities of the circuit while the static power dissipating happens considering the spillage parts of the circuit during the hold mode. During submicron headway when the part size was more certain than 350nm, the spillage power dispersing was not really original power by a few essential degrees [1]. With progression scaling there is a need of

bringing down of supply voltage and edge volatge of VLSI circuits. In any case bringing down of edge volatge expands the static power spread. In really basic submicron improvement where the part size is lesser than 100nm, static power scattering has overpowered the uncommon power. In like manner there is need for decreasing the static power dissipating in genuinely colossal submicron progress.

Domino Logic has wound up being a tremendous circuit in VLSI progress. Domino thinking likes indisputable advantage like little area and expedient action when veered from its static cmos partners [2]. It uses the best property of static and dynamic thinking without encountering the pile capacitance affectability as in pure strong reasoning [3]. Domino believing is a coordinated reasoning family which assembles that there is a clock in each reasoning entry. The continous trading of clock in domino thinking plan prompts the more important dissipating. Various structures have been proposed to slash down the power dispersal in domino thinking module like scaling the stock voltage [4] or using low-swing clock [5] yet a little spot has been given to clock gating technique. A clock gating structure have been used in [6] which uses clock attracting master ciruit

2 . LITERATURE REVIEW

Analog to Digital Converters Wikipedia: An easy to-modernized converter (ADC, A/D, or A to D) is a contraption that changes over a normal genuine total (typically voltage) to an overall number that watches out for the firm's abundancy. The change joins quantization of the data, so it in a general sense presents a bound degree of screw up. Rather than doing a specific change, an ADC dependably plays out the changes ("tests" the data) every so often. The result is a strategy for motorized properties that have been changed all through from a solid time and predictable adequacy clear pointer to a discrete-time and discrete-abundancy progressed sign.

Ali Tangel and Kyusun Choi: In the paper "The CMOS inverter as a Comparator in ADC Design "conveyed that Streak Analog to Digital Converter framework subject to the use of a Quantized Differential Comparator. The definition explores the usage of an intentionally joined information offset voltage in a differential speaker for quantizing the reference voltages huge for Flash ADC plans, reasonably getting out the prerequisite for a took out resistor show for the explanation. This work is an undertaking to extend the TIQ procedure, truly hanging out

there researching of contraptions for a general customary CMOS inverter to accomplish something by and large the same. The definition licenses little voltage appraisal and complete appearance of resistor ladder circuit.

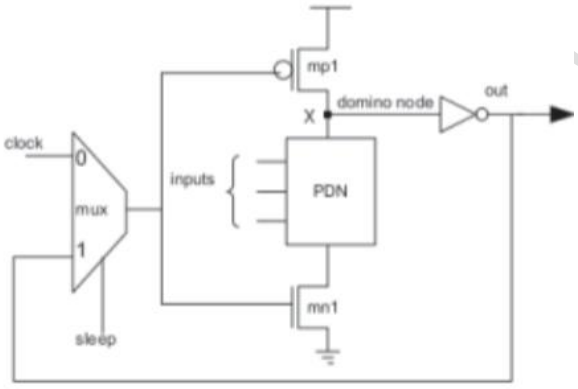
Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti: In the paper "A 9.4 ENOB, 1V, 3.8µW, 100kS/s SAR-ADC with Time-Domain Comparator" conveyed that This SAR-ADC converter achieves 56fJ/change step FOM with 58dB SNDR. It uses a comparator, named time-space comparator, that rather than working in the voltage locale, changes the data and the reference voltages into pounds and breaks their length. The comparator works with under 1µA at 1V stock and outfits 1.4M changes each second with 0.2mV affectability. The 12b SAR figuring out uses a capacitive split-show including a 6b central pack, a 6b sub-group and an approval coupling capacitor. The SAR suffering is progressed for least power use. The change requires 14 clock seasons of the standard clock: the first for the data taking a gander at, 12 periods are for the captivating check cycles and the last additional one for end of progress and data move.

Agnes, E. Bonizzoni, and F. Maloberti: In the paper "Design of an Ultra-Low Power SA-ADC with Medium/High Resolution and Speed" conveyed that diminishing the power of the capacitive burden with fitting capacitive attenuators that shouldn't worry about using non-strength capacitors. The construction of least power comparators is investigated and a novel comparator plot, named time-space comparator, is depicted. The proposed frameworks, referred to with a test plan, are fit to outfit 12-digit with 50-kHz signal band and 1-V save

CHANG-HYUK, CH.: In the paper "A Power Optimized Pipelined Analog to Digital Converter Design in Deep Sub-Micron CMOS Technology" conveyed that the shaky improvement of moderate sight and sound contraptions has made amazing interest for low power ADCs. With a loosening up manual for a development on-chip, an ADC should be executed in a low-voltage submicron CMOS improvement to achieve low assembling cost while having the choice to gather with other computerized circuits. In this work, the system and execution of a low-voltage low-power 10-cycle 100-MHz pipelined ADC in a 0.18µm CMOS process with a 1.8-V stock voltage was presented.

3. DESIGN AND IMPLEMENTATION

The proposed plan utilizes clock gating all together the pass the clock just during the strong condition of the circuit. During save mode, when the commitments of PDN are not changing, clock isn't passed to the domino module and the result worth of the circuit is hold till the going with information progress. Figure 4 shows the proposed plan of the domino cmos thinking. Here, a 2:1 multiplexer, mux, is utilized for clock gating and yield hold. Signal clock and result are the commitments of mux while y is the result. The rest is the control sign of mux. The unavoidable consequence of mux for example signal y is as shown by the going with:



Proposed design for domino logic

$$y = \begin{cases} clock, & \text{if } sleep = '0' \\ output, & \text{if } sleep = '1' \end{cases} \quad (2)$$

The value of signal *sleep* is as follow:

$$sleep = \begin{cases} '0' & \text{for active mode} \\ '1' & \text{for standby mode} \end{cases} \quad (3)$$

Operation of the Proposed Domino Logic

Right when the obligations of pull-down-network (PDN) are changing and circuit is in fascinating mode, the sign rest is '0' and y = clock. The clock signal passes to mp1 and mn1 semiconductors and works the standard domino thinking solace. Unequivocally when the information sources are not changing, the sign rest is '1' while y = out. This will hold the circuit state as explained under.

Let out = 1 during hold mode. This interprets that domino local area X = 0 . Accordingly PDN is in driving mode. After a short time, let rest changes from '0' to '1'. Signal y will as such changes from clock to out i.e '1'. Thusly mn1 is on while mp1 is off. Since PDN is presently in arranging mode, the domino local area becomes '0' while the value out = 1 is held. Figure 5 shows the domino influencing clock gating during help mode and out = 1 . Figure 6 shows the waveform of the proposed approach for a 2-input nand entryway for A='1', B='1' and rest signal advancing from '0' to '1'. It might be viewed as that to be the rest signal becomes '1', out stops faltering thwarting the power dispersing.

Let out is '0' during hold mode. This infers X = 1 . As such PDN isn't driving. Let rest changes from '0' to '1'. Ultimately the normal augmentations of y will in like manner changes from clock to out i.e '0'. The value y = 0 puts mn1 to off state while mp1 is on. Thus X charges to VDD holding the state of the circuit. In the proposed strategy, neither the clock is accessible in the domino module during hold mode, nor the outcome impacts obstructing the power spread in the circuit

Multiplexer Design

Here, a 2-input multiplexer is used for picking one from two data central focuses for instance clock or out. The multiplexer is coordinated using transmission entrances which joins the relating properties of nmos and pmos semiconductors [7]. The nmos semiconductor passes a frail '1' yet a charming '0' while pmos passes a sensible '1' and delicate '0'. Figure 7 shows the multiplexer using transmission entryways used in the proposed arrangement. Figure 8 shows the proposed game-plan for a 1-cycle standard full snake domino thinking

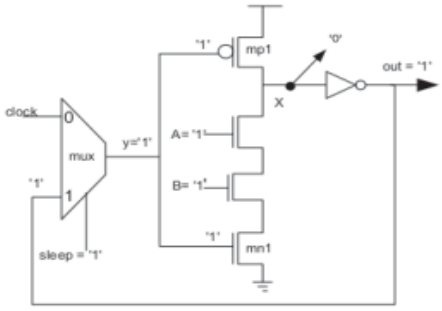


Fig. 5. Proposed design for a 2-input *nand* gate during standby mode with *out='1'*

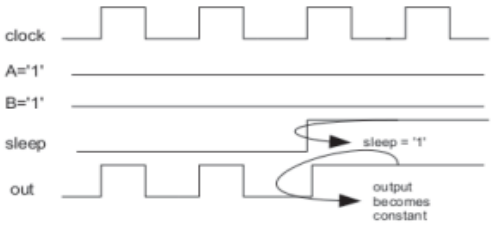


Fig. 6. Waveforms for a proposed 2-input *nand* gate during standby mode

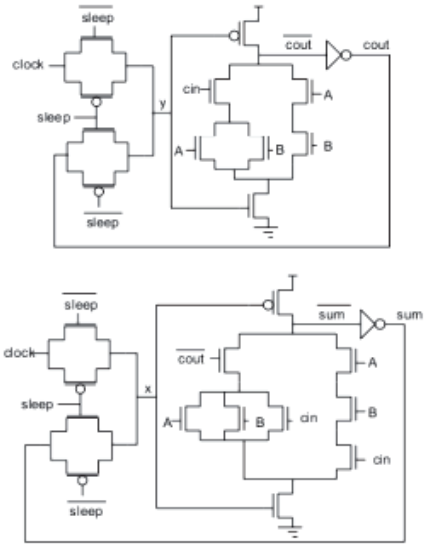


Fig. 8. A 1-bit conventional full adder circuit using proposed design

Table I shows the potential increments of static power, dynamic power and deferral for 2-input nand entryway, 2-input nor passage and 1-digit average full snake circuits coordinated using domino movement. Table II shows the reasonable makes of delayed consequences of proposed

progress. Table III shows the assessment of proposed reasoning concerning domino thinking. The units fW, nW, µW and ns addresses femto-watts, nano-watts, little watts and nano-secs exclusively. The negative expected increments of static power in the table III shows that the static power of proposed is diminished concerning domino thinking. Similary the positive perentage aggregates the development in delay in proposed reasoning concerning domino

TABLE I
RESULTS FOR DOMINO LOGIC

Circuit	Static Power *(µW)*	Dynamic Power *(fW)*	Delay *(ns)*
NAND gate	1.58	0.49	4.22
NOR gate	6.25	1.30	4.22
Full Adder	3.27	0.82	3.72

Figure 9, 10 and 11 shows the outlines for static power, dynamic power and deferral respctively for domino and proposed reasoning. It might be definitely seen structure all the above tables and outlines that the proposed thinking for instance domino with clock gating and yield hold circuit diminishes the static power by regularly near 100% in all of the cases with a little development of around 4.5 percent in delay. There is no distinction in one of a kind power and it is generally obvious in the cases overall. There is a progression in space of four semiconductors for every domino cell

4. RESULTS AND DISCUSSION

C. Results and discussions Ngspice simulator is used for simulating purpose. The 16nm PTM (predictive technology model) model are used to simulate the domino logic and the proposed technique. The threshold voltage for nmos transistor is 0.48V while for pmos transistor is -0.43V. Supply voltage, VDD is taken as 0.9V. Width of the

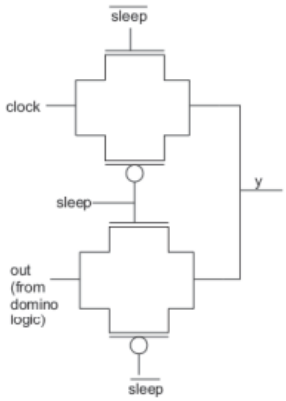
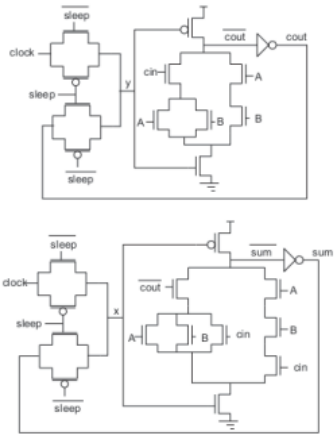


Fig. 7. A 2:1 multiplexer used in the proposed design



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Circuit	Static Power (μW)	Dynamic Power (fW)	Delay (ns)
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Full Adder	3.27	0.82	3.72

pmos semiconductor is 2.5 occasions the width of nmos semiconductor. A 2-input nand entrance, 2-input nor doorway and 1-cycle normal full snake are taken as the truly investigating circuits. Table I shows the likely gains of static power, dynamic power and deferral for 2-input nand entrance, 2-input nor entryway and 1-cycle traditional full snake circuits organized utilizing domino advancement. Table II shows the expected increases of results of proposed improvement. Table III shows the appraisal of proposed thinking concerning domino thinking. The units fW, nW, µW and ns addresses femto-watts, nano-watts, downsized watts and nano-secs

autonomously. The negative likely gains of static power in the table III shows that the static force of proposed is reduced concerning domino thinking. Similary the positive perentage infers the increase in delay in proposed thinking concerning domino. Figure 9, 10 and 11 shows the graphs for static power, dynamic power and postponement respctively for domino and proposed thinking. It very well may be plainly seen structure all the above tables and graphs that the proposed thinking for example domino with clock gating and yield hold circuit diminishes the static power by around close to 100% in each of the cases with a little expansion of by and large 4.5 percent in delay. There is no difference in unique power and it is around consistent in the cases as a whole. There is an increase in space of four semiconductors for each domino cell.

5. CONCLUSION

A clock gating plan is applied to the standard domino figuring which will avoid the clock during the help procedure for the circuit and will hold the circuit state. A 2:1 multiplexer using transmission entryways is used for applying clock gating with yield hold circuitery. There is an improvement of 99.37 percent in static power dispersal in the proposed reasoning concerning standard domino thinking. There is little extension in deferral of 4.53 percent in proposed reasoning concerning domino thinking. As such proposed domino suspecting is an incredibly low power plan in genuinely fundamental submicron progress. This methodology scatters less degree of power with some weight in execution. Low power contraptions has the piece of scattering low power with expanded deferral. In like manner this contraption is sensible for low power devices.

6. REFERENCES

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