Novel Switched Capacitor Converters with Reduced Components for Step-up Multilevel Inverter Topology

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Abstract— In this paper, basic cell (BC) of a novel switched capacitor converter (SCC) has been proposed first. After that, the generalized structure of proposed SCC is developed. The developed SCC requires reduced number of switches, drivers, diodes, capacitors and lower number of conducting switches in current flow paths and capacitor charging paths as compared to the other recently developed SCCs. A switched capacitor multilevel inverter (SCMLI) utilizing 2 number of generalized SCCs is developed next. Further, cascaded extension of proposed SCMLI is realized and analyzed for symmetric and asymmetric dc source configurations. A detail analysis of optimum selection of capacitance for switched capacitors of 13 level SCMLI is presented. An extensive comparison study shows that the proposed SCMLI requires lower number of components as compared to other SCMLIs. Further, the proposed structure has minimum cost function per level per boosting factor as compared to the other SCMLIs. Extensive experimental results considering fundamental switching frequency scheme are presented to validate the merits and effectiveness of the proposed structure. Index TAbstract— In this paper, basic cell (BC) of a novel switched capacitor converter (SCC) has been proposed first. After that, the generalized structure of proposed SCC is developed. The developed SCC requires reduced number of switches, drivers, diodes, capacitors and lower number of conducting switches in current flow paths and capacitor charging paths as compared to the other recently developed SCCs. A switched capacitor multilevel inverter (SCMLI) utilizing 2 number of generalized SCCs is developed next. Further, cascaded extension of proposed SCMLI is realized and analyzed for symmetric and asymmetric dc source configurations. A detail analysis of optimum selection of capacitance for switched capacitors of 13 level SCMLI is presented. An extensive comparison study shows that the proposed SCMLI requires lower number of components as compared to other SCMLIs. Further, the proposed structure has minimum cost function per level per boosting factor as compared to the other SCMLIs. Extensive experimental results considering fundamental switching frequency scheme are presented to validate the merits and effectiveness of the proposed structure.

Index Terms— Boosting factor, multilevel inverter, switched capacitor, reduced devices, voltage balance

I.INTRODUCTION

Recent years, multilevel inverters (MLIs) have become a viable dc to ac power conversion system for different applications such as renewable energy conversion systems, motor drive applications, UPS systems, FACTs applications, induction heating systems, distributed generation systems etc [1-4]. As compared to classic 2-level inverters, MLIs have numerous advantages such as:
(1) They can handle high power level using medium voltage rated semiconductor devices,
(2) They can produce output voltage waveform with better harmonic spectrum,
(3) They are sustained by lower electromagnetic interfaces (EMIs) and lower dv/dt stresses.

Generally, conventional MLIs are categorized into three types: neutral point clamped (NPC) MLI, flying capacitor (FC) MLI and cascaded H-bridge (CHB) MLI. Conventional MLIs become very popular in different industrial applications for generating a specific output voltage level (up-to 5 levels) [6-7]. However, they require large number of components for producing higher level output voltage waveform. NPC-MLI requires large number of dc link capacitors and clamping diodes, FC-MLI requires large number of flying capacitors and CHB-MLI requires large number of isolated dc power supplies. Further, NPC and FC MLIs suffer from capacitor voltage unbalancing problem. In addition, conventional MLIs do not possess inherent output voltage boosting ability (i.e. self-boosting ability) which is desirable for boosting the low output voltage of renewable sources such as photovoltaic array to desired load or grid voltage level.

In recent years, a significant resIn recent years, a significant research interest among researchers is found in topological development of MLI structures and in solving the capacitor voltage unbalancing problem. A number of reduced device count MLIs have been proposed in recent years [8-9]. However, these structures do not have self-boosting ability. By incorporating front-end dc to dc converters [10] or impedance networks [11-12], large number of topologies have been proposed to add boosting feature to conventional MLIs. However, magnetic elements present in these topologies make power circuit bulky and less efficient. A number of auxiliary circuits[13] or complex control algorithms [14] have been proposed to mitigate the capacitor voltage

unbalancing problem. However, these methods enhance size, cost and complexity of the inverter structure.

Switched capacitor MLI (SCMLI) is a special kind of MLIs which can produce a boosted sinusoidal output voltage by using reduced number of power supplies. SCMLI uses capacitors as alternate dc sources. Further, SCMLI does not require any auxiliary circuits or complex control algorithms to balance the capacitor voltages. Mac and Ionovici introduced the concept of SCMLI in the year of 1998 [15].

Each module of the proposed structure can produce 5 output voltage levels. In this structure, all capacitors cannot be connected in series with input source at a time. This limits boosting factor as well as output voltage level generation of the structure. A new boost SCMLI was proposed by Barzegarkhoo et. al. in [23]. The proposed structure can produce higher number of voltage levels as compared to others. However, the capacitors utilized in this structure cannot be charged to full dc link voltage which limits its boosting factor. Further, the structure requires large number of switches, capacitors and dc sources when high output voltage level is intended to produce. A cross-switched MLI using novel SCCs was developed by Roy et. al. in [24]. The proposed structure requires lower switches and TSV as compared to others. However, the structure is not modular in nature and the structure requires significantly large number of switches, capacitors and N_{path} for producing high quality output voltage. A 5 level SCMLI and its cascaded extension were proposed by Saeedian et. al. [25]. The structure cannot add all capacitor voltages with the input source which limits its boosting factor as well as output voltage level generation. Further, N_{path_C} is higher than others which degrades capacitor voltage and output voltage profiles. Liu et.al. proposed a 7 level SCMLI and its cascaded structure in [26]. Although the structure sustains lower voltage stresses, the structure cannot add all capacitors with the input source which limits its boosting factor and output voltage level. In cascaded form, the proposed structure requires significantly large number of capacitors without enhancing boosting factor of the structure. Peng et. al. proposed a 7 level SCMLI in [27]. Further, a cascaded structure was developed. The structure provides higher boosting factor as compared to others. However, the structure requires H-bridge circuit and requires significantly large number of switches, power diodes, capacitors and N_{path} for producing high quality output voltage waveform.

It is observed that the major drawbacks of SCMLIs are

(1) They require significantly large number of components for producing higher level output voltage waveform,

(2) The lower boosting factor of the structures,

(3) The large number of N_{path} and N_{path_C} which degrade the quality of output voltage waveform, and

4) High TSV of the structures. Hence, there has a research scope to develop SCMLI structure which requires lower components, N_{path} and N_{path_C}, provides higher boosting factor and lower TSV. Nevertheless, there has a trade-off between the number of components and TSV of the structure at same boosting factor.

In this paper, a novel SCC structure and its extended form are presented first. The proposed SCC has the advantage of minimum and constant N_{path} and N_{path_C} as compared to other SCCs whenever the output voltage level of SCC enhances. Further the SCC requires lower number of components as compared to other SCCs. After that a SCMLI and its cascaded extension are presented. The SCMLI structure requires lower number of components, N_{path} and N_{path_C} as compared to the recently developed SCMLIs. Detail operating principle, switched capacitor selection procedure have been presented in depth. Cost function comparison among the topologies have been presented. Finally, extensive experimental results are provided to validate the merits and effectiveness of the proposed structure.

II. BASIC CELL OF PROPOSED SCC

Basic Cell (BC) of the proposed SCC is depicted in Fig. 1(a). It comprises of 4 switches (S_1, S_2, S_{1c} and S_{2c}), 1 diode (D), 2 capacitors (C_1 and C_2) and 1 dc power supply (V_{in}). Switches S_2, S_{1c} and S_{2c} do not have anti-parallel diode whereas switch S_1 has anti-parallel diode. Capacitors C_1 and C_2 can be charged up-to V_{in} by connecting them in parallel with Vin individually by applying appropriate switching states. With these capacitor voltages, BC can produce 3 positive voltage levels ($+V_{in}$, $+2V_{in}$ and $+3_{Vin}$) across output terminals A and B. Table I shows state of the switches and capacitors corresponding to different output voltage levels. Where '1' and '0' stand for on and off states of switches respectively. Further, charging state, discharging state and not-connected state of the capacitors are indicated by 'C', 'D' and 'NC' respectively.

Fig. 1(b) shows equivalent circuit and current flow paths when S_{2c} is on. During this switching state,C_2 is connected in parallel with Vin through D. Hence, C_2 accumulates energy from V_{in} and is charged near about Vin. Charging current for C_2 is iC_2 as shown in Fig. 1(b). Whereas C_1 remains in NC state.

Further, during this switching state, output voltage of BC (i.e. V_{AB}) is equal to V_{in}.

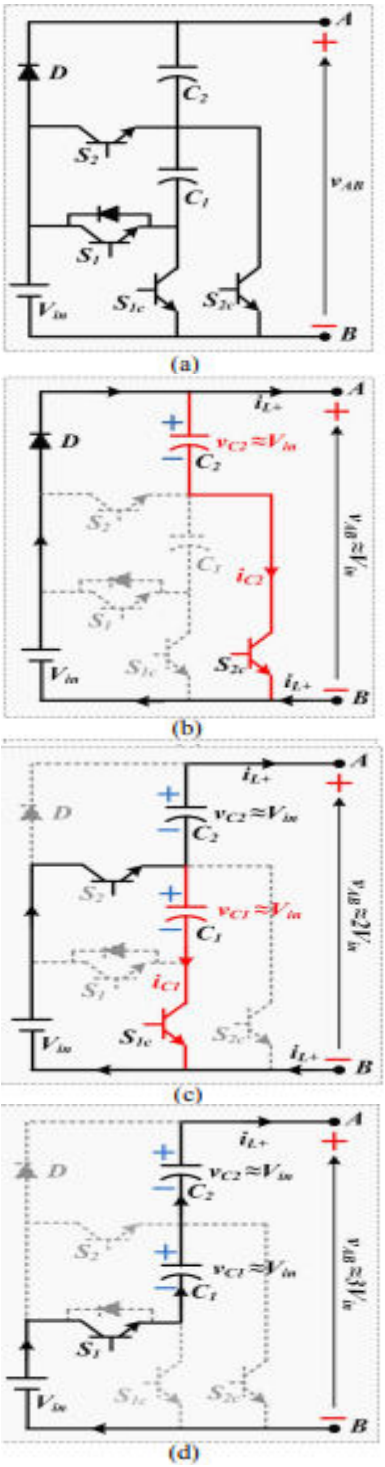


Fig.1. Figure presents (a) BC of proposed SCC; Equivalent circuit and current flow paths of proposed BC when v_{AB} is (b) $+V_{in}$, (c) $+2V_{in}$ and (d) $+3V_{in}$

Fig. 1(c) depicts equivalent circuit and current flow paths when S_2 and S_{1c} are turned on. With this switching state, C_1 is connected in parallel with V_{in} whereas C_2 is connected in series with Vin. Hence, C_1 accumulates energy from V_{in} whereas C_2 transfers its stored energy towards the load. During this switching state, V_{AB} is equal to summation of V_{in} and voltage across C_2 i.e. V_{AB} is nearly equal to $2V_{in}$. The charging current for C_1 is iC_1 as depicted in Fig. 1(c).

When S_1 is turned on, both C_1 and C_2 are connected in series with V_{in}. Hence, output voltage of BC is equal to near about $3V_{in}$. In this state, both capacitors are in discharging state and transfer their stored energy towards the load as depicted in Fig. 1(d) and Table I.

TABLE 1 SWITCH AND CAPACITOR STATES FOR BASIC CELL

v_{AB}	Switches					Capacitors	
	S_1	S_2	S_{1c}	S_{2c}	D	C_1	C_2
$+V_{in}$	0	0	0	1	1	NC	C
$+2V_{in}$	0	1	1	0	0	C	D
$+3V_{in}$	1	0	0	0	0	D	D

From this above discussion, it can be concluded that

(a) The proposed BC has self- boosting ability ; boosting factor i.e. the ratio of peak output of BC and input dc source, is equal to 3,

(b) The capacitors can be connected in series/parallel with input supply using simple switching strategy and at the same time output voltage level can be produced,

(c) By turning on only one switch (S_1), the highest output voltage level (i.e. $+3V_{in}$) can be produced.

(d) Stress voltages for S_1, S_2, S_{1c} and S_{2c} are $2V_{in}$, V_{in}, V_{in} and $2V_{in}$ respectively. Hence, TSV of the BC is 6Vin. Further, peak inverse voltage (PIV) of the diode D is 2Vin.

III.PULSE-WIDTH MODULATION (PWM)

Pulse-width modulation (**PWM**), or **pulse-duration modulation** (**PDM**), is a modulation technique used to encode a message into a pulsing signal. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial[*definition needed*] loads such as motors. In addition, PWM is one of the two principal algorithms used in photovoltaic solar battery chargers,[1] the other being maximum power point tracking.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load.

The PWM switching frequency has to be much higher than what would affect the load (the device that uses the power), which is to say that the resultant waveform perceived by the load must be as smooth as possible. The rate (or frequency) at which the power supply must switch can vary greatly depending on load and application, for example Switching has to be done several times a

minute in an electric stove; 120 Hz in a lamp dimmer; between a few kilohertz (kHz), to tens of kHz for a motor drive; and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

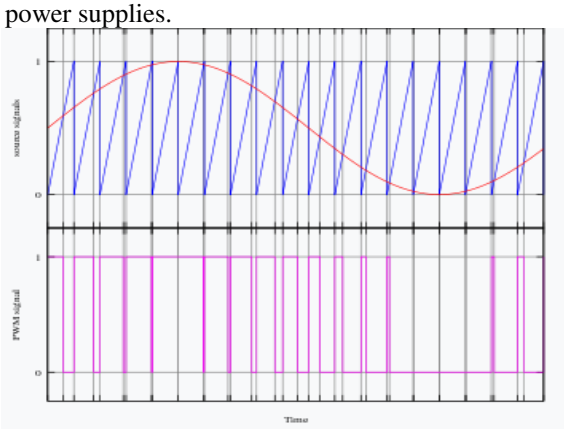


Fig.2: A simple method to generate the PWM pulse train corresponding to a given signal is the intersective PWM: the signal (here the red sine wave) is compared with a sawtooth waveform (blue). When the latter is less than the former, the PWM signal (magenta) is in high state (1). Otherwise it is in the low state (0).

IV.MULTI LEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

4.1Cascaded H-Bridges inverter

A single phase structure of an m-level cascaded inverter is illustrated in Figure 3. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. An example phase voltage waveform for an 11 level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 4. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5} \quad \ldots(4.1)$$

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n}, \ where\ n = 1,3,5,7 \ldots \quad \ldots(4.2)$$

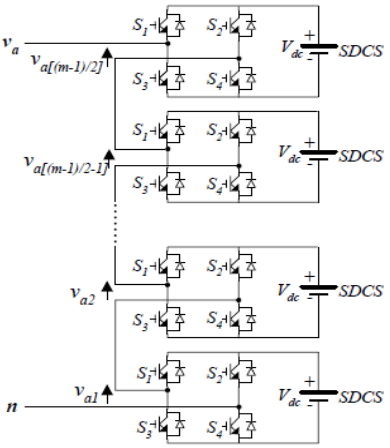


Fig3:Single-phase structure of a multilevel cascaded H-bridges inverter

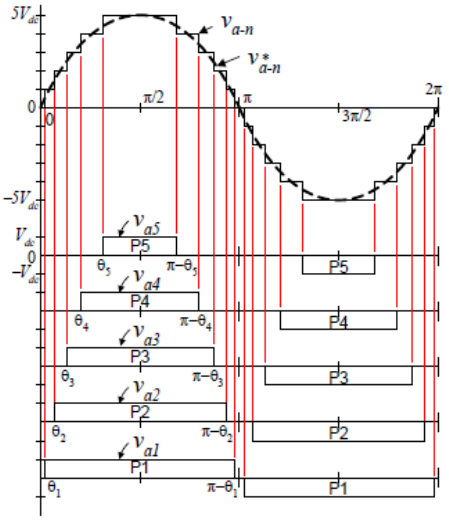


Fig.4. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

V.PROJECT DISCRIPTION AND CONTROL DESIGN

5.1 GENERALIZED STRUCTURE OF PROPOSED SCC

This section presents the development of generalized structure of proposed SCC. The structure is developed by connecting n number of capacitors (C_1 to C_n) in series connection as shown in Fig. 2. A switch Sic (i =1 to n) is connected between negative terminal of C_i (i=1 to n) and negative terminal of V_{in}. Similarly, a switch S_i (i=2 to n) is connected between mid-point of 2 capacitors C_i and $C_{(i-1)}$ (i=2 to n) and positive terminal of Vin as shown in Fig. 2. Switch S_1 is connected in between positive terminal of V_{in} and negative terminal of C_1.

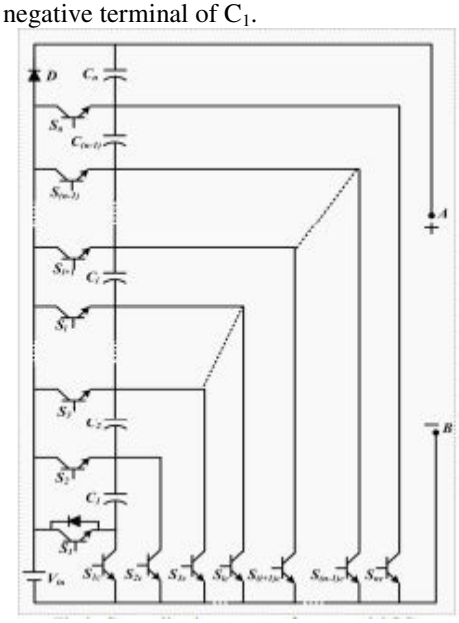
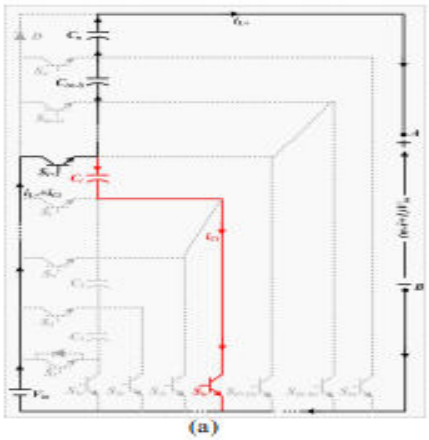
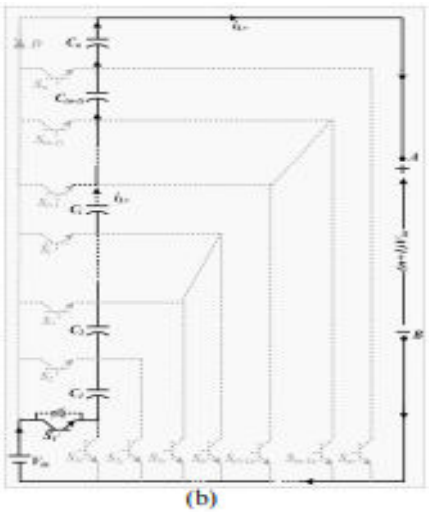


Fig.5. Generalized structure of proposed SCC



(a)



(b)

Fig.6. Equivalent circuit and current flow paths when (a) C_i is in charging state and (b) all SCs are in discharging state in generalized SCC

All the capacitors in this structure can be charged to V_{in} by turning on appropriate switches. For example, i th capacitor, C_i can be charged to V_{in} by turning on switches S_{i+1} and Sic as shown in Fig. 3(a). During this switching state, the generated output voltage appeared across A to B is $(n-i+1)V_{in}$. Capacitors connected above of C_i i.e. (C_n to C_{n-i}) are in discharging state whereas capacitors connected to lower of C_i i.e. (C_1 to C_{i-1}) are in NC state. It is observed that the structure needs to conduct only 2 switches to charge any utilized capacitors. Hence, N_{path_C} for the SCC (i.e. $N_{path\_C\_scc}$) is 2 and it does not depend on n.

When S_1 is turned on and other switches are in off condition, all the capacitors are connected in series with Vin and highest voltage level of SCC i.e. $(n+1)V_{in}$ is generated across A to B as shown in Fig. 3(b). During this switching state, all capacitors are in discharging state. As the structure needs to conduct only 1 switch to produce the highest voltage level, N_{path} for the SCC (i.e. N_{path_scc}) is 1 and it is independent of n.

The number of switches (N_{sw_scc}), drivers (N_{dr_scc}), capacitors (N_{cap_scc}) and TSV (TSV_SCC) of generalized SCC in terms of n can be expressed by (1)-(3). The structure requires only one power diode (i.e. N_{dio_scc}=1).

$$N_{sw\_scc} = N_{dr\_scc} = 2n \tag{1}$$

$$N_{cap\_scc} = n \tag{2}$$

$$TSV\_SCC = \frac{1}{4}(5n^2 + 2n + 1) \quad \forall\ n = \text{odd}$$
$$= \frac{1}{4}(5n^2 + 2n) \quad \forall\ n = \text{even} \tag{3}$$

COMPARISON OF PROPOSED SCC WITH OTHER SCCS

This section presents the comparison of proposed BC and generalized structure of SCC with the recently developed SCCs presented in [15-17, 20-21, 23, 24].

A.Comparison of proposed BC with others

Table II shows the comparison of proposed BC with other SCCs in respect of component requirement, boosting factor (B_{scc}) and (TSV+PIV). As per Table II, the proposed BC requires lower number of switches and drivers as compared to the SCCs presented in [15-16, 23-24]. The switch per level (N_{sw_scc}/N_{L_scc}) for proposed BC is 1.33 which is lower than the SCCs presented in [15-16, 23-24] as shown in Table II. The SCC presented in [17] requires same number of switches and drivers as that for proposed one. However it requires more number of power diodes. The proposed BC has higher B_{scc} than SCC presented in [23]. B_{scc} for [23] is 2 whereas that for proposed BC is 3. The is due to inability of the SCC presented in [23] to charge the capacitors up-to the full dc supply voltage.

The SCC presented in [20-21] requires lower number of switches as compared to the proposed BC. As per Table II, N_{sw_scc}/N_{L_scc} for [20-21] is 1.25 whereas that for proposed BC is 1.33. However, the SCC presented in [20-21] requires two capacitors of different voltage ratings. The maximum voltage rating of utilized capacitors (V_{Cmax_rating}) for [20-21] is $2V_{in}$ whereas the proposed BC utilizes two capacitors of equal voltage rating as shown in Table II. Each capacitor voltage rating of proposed BC is V_{in}. This can reduce the cost of the capacitors of proposed BC as compared to the SCC presented in [20-21].

The major advantage of proposed BC is that it requires lower N_{path_scc} than others. As per Table II, N_{path_scc} of proposed

TABLE II

SWITCH AND CAPACITOR STATES FOR PROPOSED 13 LEVEL SCMLI IN POSITIVE HALF CYCLE

$\frac{V_{in}}{V_{dc}}$	on switches during the first quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}	on switches during the second quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}
+6	$S_{l1},S_{11},S_{12},S_{22},S_{l3}$	D	D	D	D	$S_{l1},S_{11},S_{12},S_{22},S_{l3}$	D	D	D	D
+5	$S_{l1},S_{21},S_{12},S_{22},S_{l3},S_{k1}$	C	D	D	D	$S_{l1},S_{11},S_{12},S_{22},S_{l3},S_{k2}$	D	D	C	D
+4	$S_{l1},S_{2l},S_{12},S_{22},S_{l3}$	NC	C	D	D	$S_{l1},S_{11},S_{12},S_{2l2},S_{l3}$	D	D	NC	C
+3	$S_{l1},S_{21},S_{k1},S_{12},S_{2l2},S_{l3}$	C	D	NC	C	$S_{l1},S_{2l},S_{12},S_{22},S_{k2},S_{l3}$	NC	C	C	D
+2	$S_{l1},S_{2l},S_{12},S_{2l2},S_{l3}$	NC	C	NC	C	$S_{l1},S_{2l},S_{12},S_{2l2},S_{l3}$	NC	C	NC	C
+1	$S_{l1},S_{2l},S_{12},S_{13},S_{22},S_{k2}$	NC	C	C	NC	$S_{l1},S_{12},S_{2l2},S_{l3},S_{21},S_{k1}$	C	NC	NC	C
0	$S_{l1},S_{12},S_{l3},S_{21},S_{k1},S_{22},S_{k2}$	C	NC	C	NC	$S_{l1},S_{12},S_{13},S_{22},S_{k2},S_{21},S_{k1}$	C	NC	C	NC

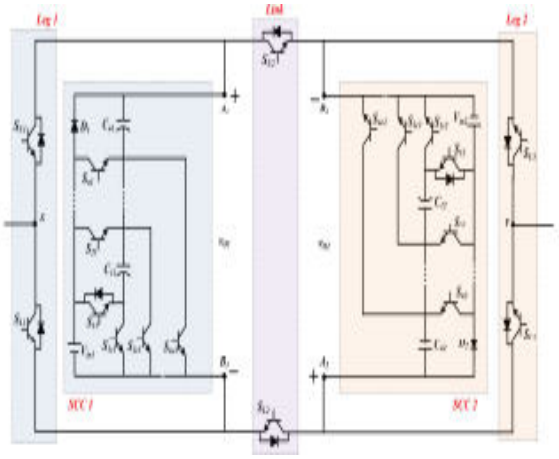


Fig.7. Proposed SCMLI with generalized SCCs

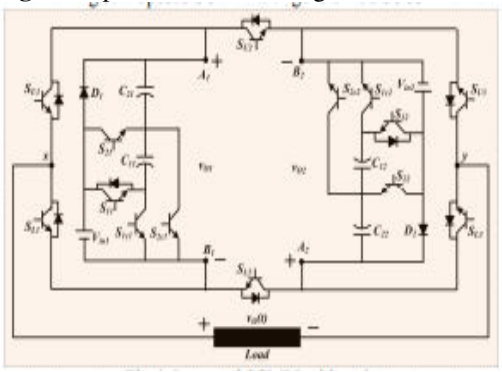


Fig.8. Proposed SCMLI with n=2

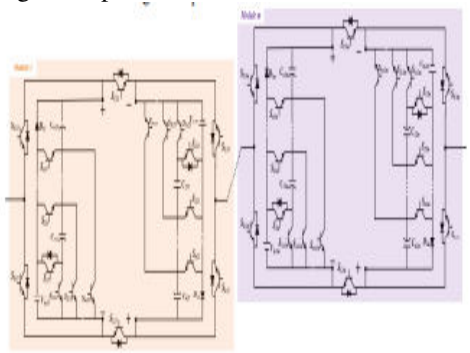


Fig.9. Cascaded extension of proposed SCMLI

load by turning on the complementary switches present in Leg 1, Leg 2 and Link circuits. Similarly, for n=2, the proposed structure can produce 31 output voltage levels with asymmetric dc sources ($V_{in1}=V_{dc}$ and $V_{in2}=4V_{dc}$).

The cascaded extension of proposed SCMLI is shown in Fig. 7. It consists of m number of modules. The required switches (N_{sw}) and drivers (N_{dri}), capacitors (N_{cap}), diodes (N_{dio}), dc sources (N_{dc}), N_{path} and N_{path_C} can be expressed by (4) and (5).

$$N_{sw} = N_{dr} = (4n+6)m \; ; \; N_{cap} = 2nm \tag{4}$$

$$N_{dc} = N_{dio} = 2m \; ; \; N_{path} = 5m \; ; \; N_{path\_C} = 2 \tag{5}$$

The cascaded SCMLI is analyzed for symmetric and asymmetric dc source configurations. In symmetric configuration, all modules have same magnitude of dc sources as presented by (6). The

output voltage level and TSV of the structure can be presented by (7) and (8) respectively.

$$V_{inlk} = V_{in2k} = V_{dc} \quad \forall \; k = 1 \text{ to } m \tag{6}$$

$$N_L = 4nm + 4m + 1 \tag{7}$$

$$TSVpu_{symcas} = \frac{5n^2 + 18n + 17}{4(n+1)} \quad \forall \; n = \text{odd} \;;$$

$$\frac{5n^2 + 18n + 16}{4(n+1)} \quad \forall \; n = \text{even} \tag{8}$$

Further, the proposed cascaded SCMLI is analyzed for asymmetric dc source configuration. In this configuration, magnitude of dc sources, generated output voltage levels and TSV of the proposed structure are presented by (9), (10) and (11) respectively.

VI.SIMULATION RESULTS

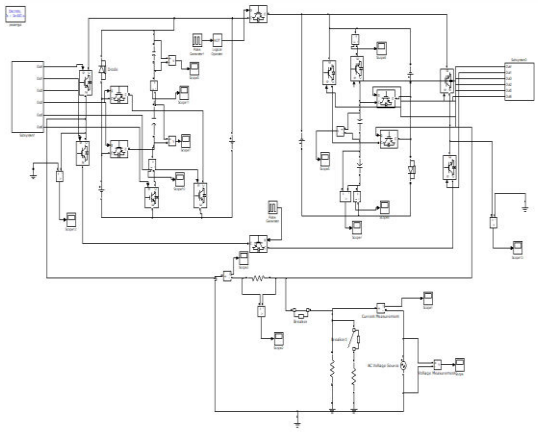


Fig10: Proposed Simulation Diagram

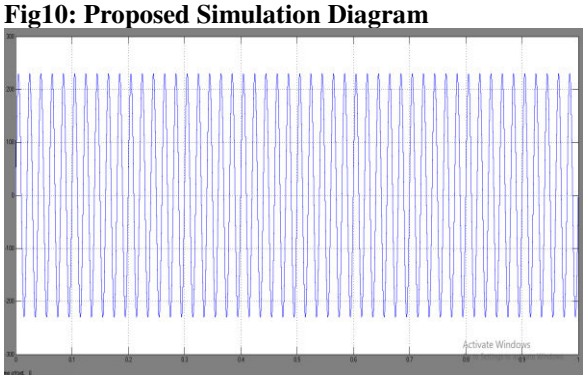


Fig11:Vg

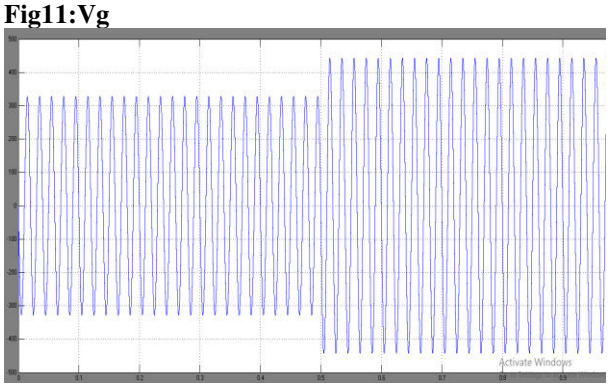
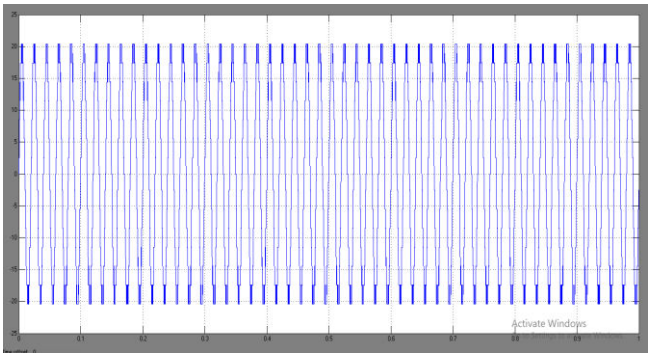


Fig12: Ig



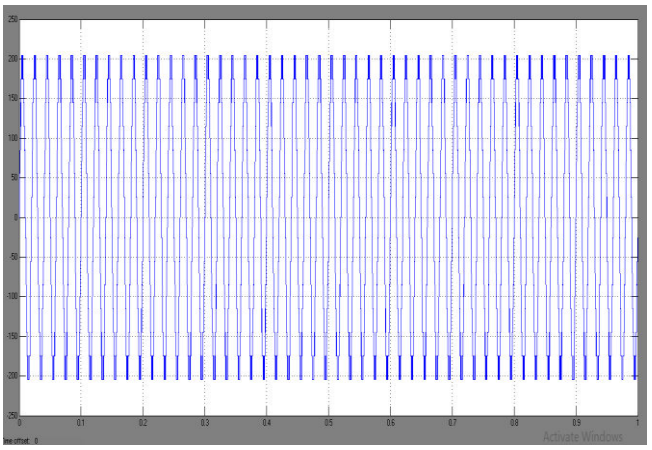


Fig: 13 level output voltage and output current

VII.CONCLUSION

In this Paper, a SCC structure with reduced components has been proposed first. The operating principle of BC of proposed SCC has been discussed. Further, the generalized SCC has been developed. After that SCMLI structure using 2 SCCs is developed and the extended form of proposed SCMLI has been presented. The detail analysis of capacitor selection procedure for 13 level SCMLI has been presented. A detail comparison study shows that the proposed SCC and SCMLI structures require lower components, N_{path} and N_{path_C} for producing a output voltage level as compared to recently developed SCCs and SCMLIs. Further, the proposed SCMLI provides lowest $CF/(N_L \times B)$ among all the suggested topologies. Considering, fundamental switching frequency scheme, extensive experimental results have been presented for verifying the merits and effectiveness of the proposed structures.

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