MODIFIED HIGH SPEED 32-BIT VEDIC MULTIPLIER DESIGN AND IMPLIMENTATION

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ABSTRACT

The proposed research work specifies the modified version of binary Vedic multiplier using Vedic sutras of ancient Vedic mathematics. It provides modification in preliminarily implemented Vedic multiplier. The modified binary Vedic multiplier is preferable has shown improvement in the terms of the time delay and also device utilization. The proposed technique was designed and implemented in Verilog HDL. For HDL simulation, Xilinx tool is used and for circuit synthesis, Xilinx is used. The simulation has been done for 4 bit, 8 bit,16 bit,32 bit multiplication operation. Only for 32 bit binary Vedic multiplier technique the simulation results are shown. This modified multiplication technique is extended for larger sizes.

Index Terms—Vedic multiplier, Kogge stone adder, Verilog HDL, simulation, synthesis.

INTRODUCTION

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics can be aptly employed here to perform multiplication.

MULTIPLIER

A binary multiplier can be used in digital electronics as a electronic circuit, such as in computers to find the product of two binary numbers. Carbon-copy of normal multiplication technique is used by binary multiplier, the multiplicand is multiplied with each bit of the multiplier beginning from the least significant bit. Two half adder(HA) modules can be used in order to implement a 2-bit binary multiplier. A no of computer arithmetic calculations can be used to appliance digital multiplier. Among these techniques many imply computing a set of partial products, and then summing the generated partial products together. Fig. 1, shows 2x2 binary multiplier.

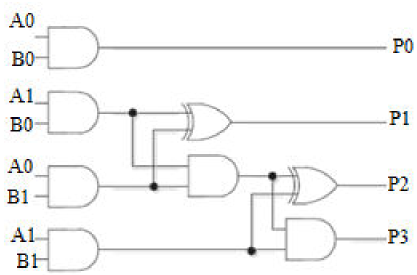

Fig1: 2x2 Vedic multiplier

1. LITERATURE SURVEY

Vijay Kumar Reddy Modified High Speed Vedic Multiplier Design and Implementation The proposed research work specifies the modified version of binary Vedic multiplier using Vedic sutras of ancient Vedic mathematics. It provides modification in preliminarily implemented Vedic multiplier. The modified binary Vedic multiplier is preferable has shown improvement in the terms of the time delay and also device utilization. The proposed technique was designed and implemented in Verilog HDL. For HDL simulation, modalism tool is used and for circuit synthesis, Xilinx is used. The simulation has been done for 4 bit, 8 bit, 16 bit, multiplication operation. Only for 16 bit binary Vedic multiplier technique the simulation results are shown. This modified multiplication technique is extended for larger sizes. The outcomes of this multiplication technique is compared with existing Vedic multiplier techniques.

2. MODIFIED VEDIC MULTIPLIER

In the proposed paper, the two parallel adders are replaced by KSA [4] for the better execution of the multiplier architecture. The recommended modified Vedic multiplication methodology is done in the following for 4 bit inputs, A(A3-A0) and B(B3 -B0) and 8 bit output S (S7 -S0).

$A_3A_2A_1A_0$

x $B_3B_2B_1B_0$

$(A_3A_2)x(B_1B_0)$ $(A_1A_0)x(B_1B_0)$

$(A_3A_2)x(B_3B_2)$ $(A_1A_0)x(B_3B_2)$

S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0

A multiplier of 2 bit is used to calculate intermediate stage results, and the output is 4 bits. (A3A2)(B3B2) using 2 bit multiplier generates result: S33S32S31S30

(A3A2)(B1B0) using 2 bit multiplier generates result: S23S22S21S20

(A1A0)(B3B2) using 2 bit multiplier generates result: S13S12S11S10

(A1A0)(B1B0) using 2 bit multiplier generates result: S03S02S01S00

The mode used by Vedic multiplier is Vedic mathematics. By using this technique it will increase, and consumes fewer hardware elements. The sutra used by Vedic multiplier is Urdhva Tiryakbhyam which means Vertically as well as Crosswise. The Fig. 3 shows block diagram of 32 bit Vedic multiplier circuit. The2 input bits are separated into 2 similar parts the vertical and cross product calculations can be done as shown in Fig. 3, with inputs A[31:0] and B[31:0].As shown in the Fig. 3, the 2 adders are used in the design of intermediate stages of the addition. The output carry Cout from these two adders is given as input to another KSA. If bits are not of equal sizes concatenate them. For 32-bit Modified Vedic multiplier the outputs of parallel adder is given to OR gate and of the size of last KSA is reduced to half. Fig. 3, shows 32-bit Vedic multiplier.

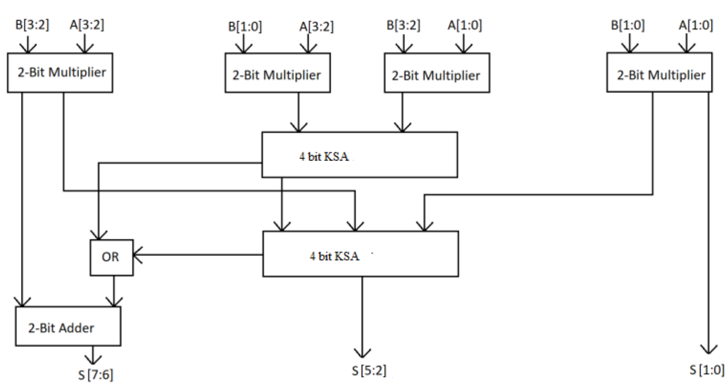

Fig2: 4 Bit Vedic multiplier using KSA

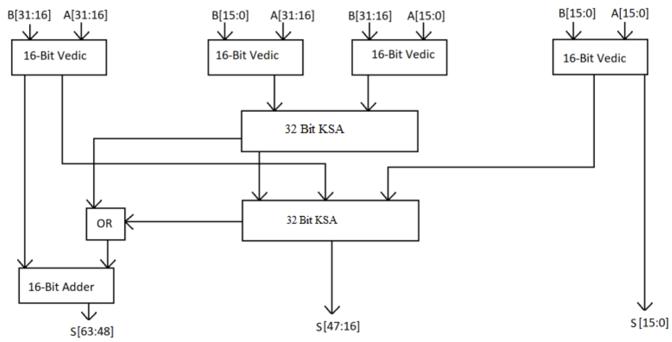

Fig3: 32 Bit Vedic multiplier using KSA

KOGGE STONE ADDER

KSA is a parallel prefix form carry look ahead adder. It generates carry in O (logn) time and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits. In KSA, carries are computed fast by computing them in parallel at the costof increased area. The complete functioning of KSA can be easily comprehended by analyzing It in terms of three distinct parts :

1. Pre processing

This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B.

pi = Ai *xor* Bi

gi = Ai *and* Bi

2 . Carry look ahead network

This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit . It uses group propagate and generate as intermediate signals .

Pi:j = Pi:k+1 *and Pk:j*

Gi:j = Gi:k+1 *or* (Pi:k+1 *andGk:j*)

3. Post processing

This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits.

Si = pi xor Ci-1

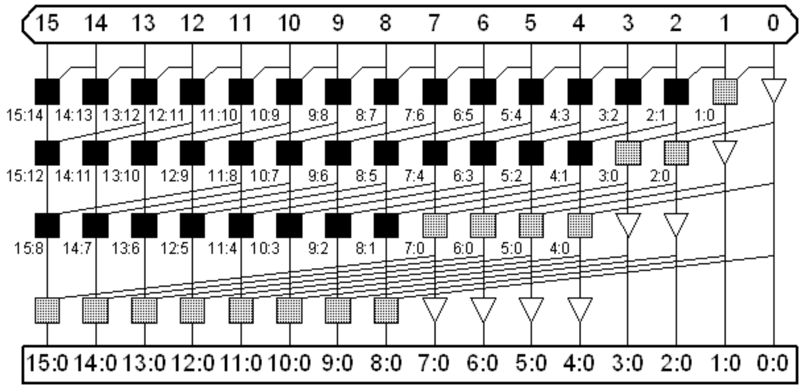

Fig4 : 16 bit kogge stone adder

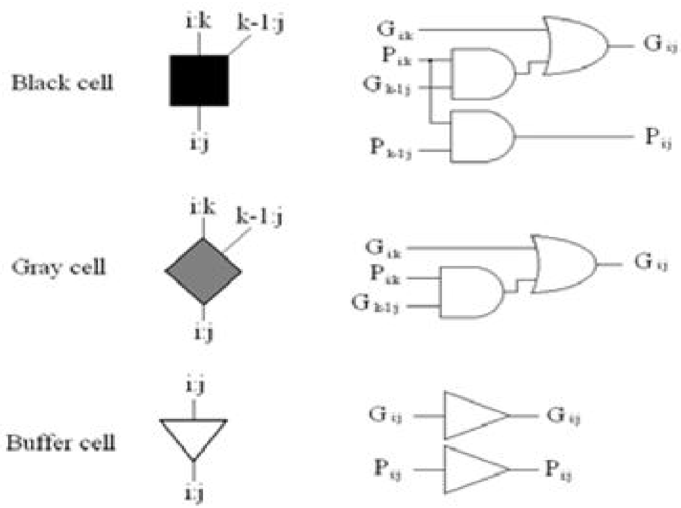

Fig 5: Complex logic cells inside the Prefix Carry Tree

RESULTS

RTL SCHEMATIC: The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development .The HDL language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e Verilog,VHDL. The RTL schematic even specifies the internal connection blocks for better analyzing .The figure represented below shows the RTL schematic diagram of the designed architecture.

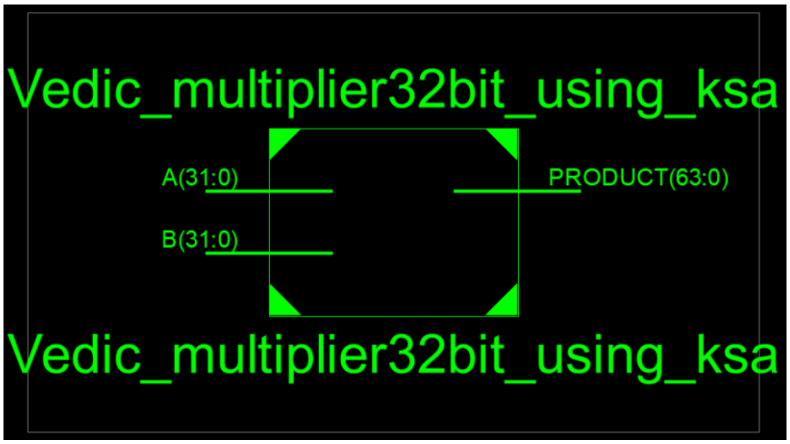

Fig6: RTL Schematic of Vedic multiplier using KSA

TECHNOLOGY SCHEMATIC: The technology schematic makes the representation of the architecture in the LUT format ,where the LUT is consider as the parameter of area that is used in VLSI to estimate the architecture design .the LUT is consider as an square unit the memory allocation of the code is represented in there LUT s in FPGA.

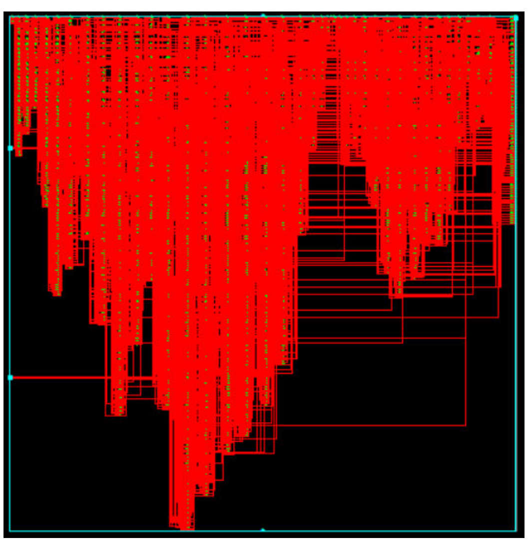

Fig7: View Technology Schematic of Vedic multiplier using KSA

SIMULATION: The simulation is the process which is termed as the final verification in respect to its working where as the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implantation to the simulation on the home screen of the tool, and the simulation window confines the output in the form of the wave forms. Here it has the flexibility of providing the different radix number systems.

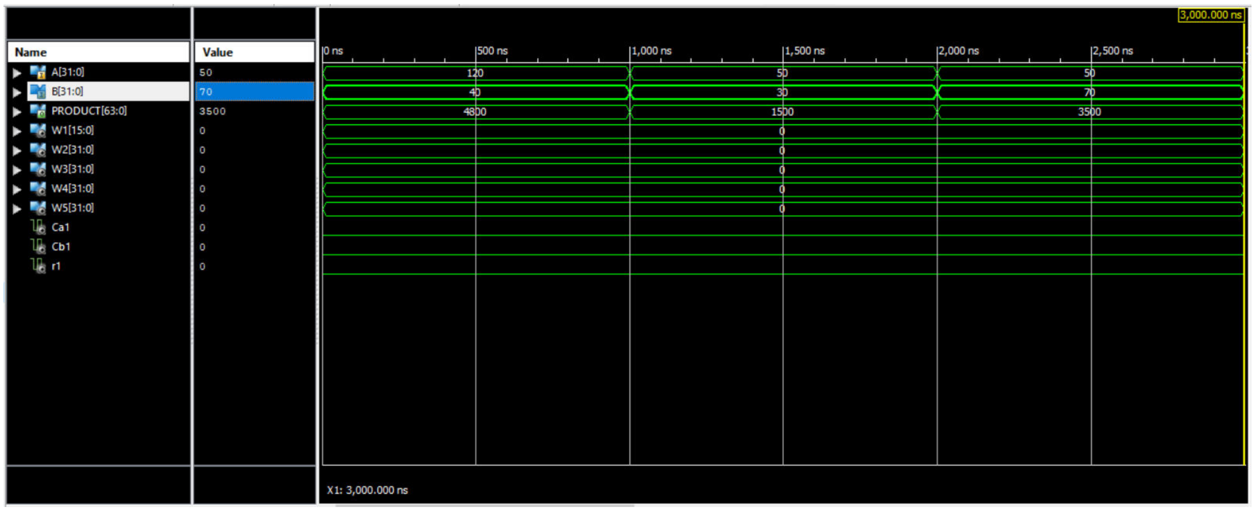

Fig8 : Simulated Waveforms of Vedic multiplier using KSA

PARAMETERS: Consider in VLSI the parameters treated are area ,delay and power ,based on these parameters one can judge the one architecture to other. Here the consideration of delay is considered the parameter is obtained by using the tool XILINX 14.7 and the HDL language is verilog language.

Parameter	Vedic multiplier using CSA	Vedic multiplier using KSA
No of LUTs	2835	2834
Delay (ns)	24.659	20.061

Table 1: parameter comparison table

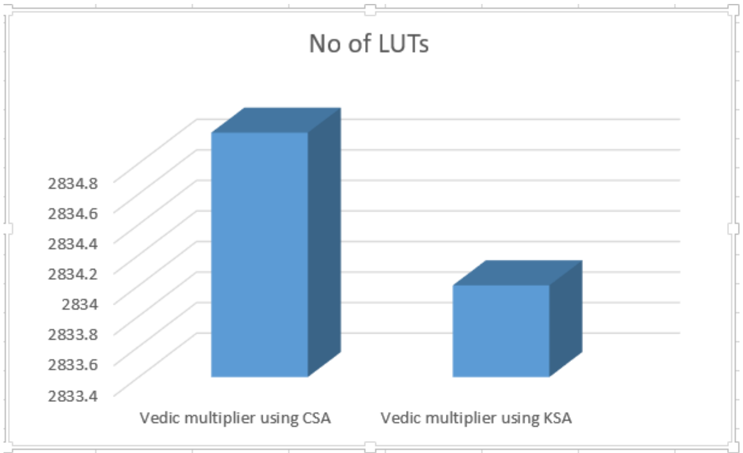

Fig9 : LUT comparison bar graph

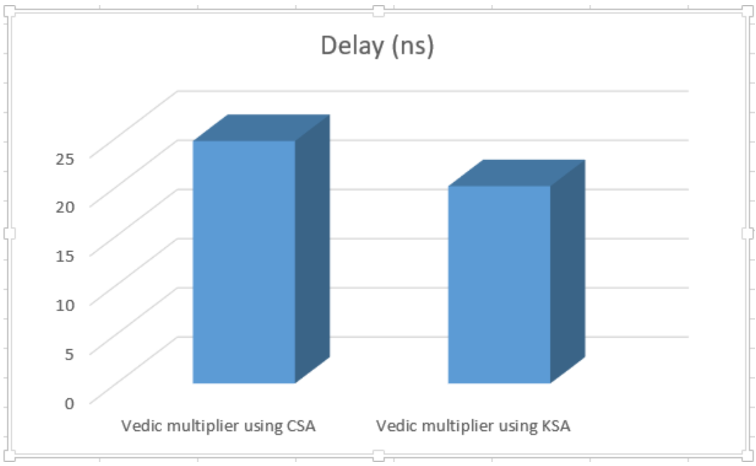

Fig 10: Delay comparison bar graph

CONCLUSION

This paper has presented a systematic method for binary multiplier circuits which is based on Vedic mathematics. When it comes to the terms of time delay then the proposed system is more efficient than exisitng methods. Elongation for a higher bit size can be done with help of proposed technique. Moreover, adders of different architectures can be used in the kogge Stone Adder design used in the proposed modified Vedic multiplier. Among many techniques modified architecture is used to increase and speed up the multiplication.

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