DESIGN AND ANALYSIS OF LINEAR FEEDBACK SHIFT REGISTER BASED CONDITIONAL DISCHARGE FLIP-FLOP (CDFF) AND GATE-DIFFUSION-INPUT (GDI) TECHNIQUE

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ABSTRACT: The Linear Feedback Shift Register's input bit is a linear function of previous state output. The conventional way of implementing LFSR is done by combining flip-flop and XOR gate. The objective of GDI is reduction of transistors count, low power dissipation and simple gates. LFSR is combination of flip-flop and XOR gate. Our proposed system is a combination of GDI and CDFF techniques as discussed earlier. XOR gate is implemented using GDI and flip-flop is implemented using conditional discharge technology. A new design of the Linear-feedback shift register (LFSR) using the conditional discharge flip-flop (CDFF) and the Gate-Diffusion-Input (GDI) technique is proposed. This method results in efficient result parameters such as low power, reduced area and minimum usage of transistor than conventional techniques. With respect to the above parameters, other LFSR designing technique's performance is compared and presented. The resultant bits from LFSR are usually sampled for n-bit random number generation. Most importantly complexity of the design is very simple.

1. INTRODUCTION

In the view of generating a pseudo-random pattern, Linear Feedback Shift Registers are foremost. The Linear Feedback Shift Register's input bit is a linear function of previous state output. The conventional way of implementing LFSR is done by combining flip-flop and XOR gate, the advancements and the changes made to the existing methods are discussed here. To discuss other methods of implementation, GDI stands unique for its minimized number of transistors. Size is the most considerable parameter in the eyes of VLSI devices, Gate Diffusion Input is one of the impressive technique in the aspect of the size of transistor and area. The GDI is an alternative logic design in the standard CMOS technologies. Structure of GDI are discussed below, where Fig1 shows the simple GDI cell.

In complementary metal oxide semiconductor circuit based designs, flip-flops are essential part of the clocking circuits. They are responsible for the synchronous-asynchronous behavior to the system. The basic circuit of flip flop that is used in various digital circuits determines the system power consumption. The type of flip flop used in digital circuits determines the output load of the circuits. This is also known as clock load. This clock load directly affects the switching power consumption of circuits. Therefore, it is essential to introduce one technique to minimize the power consumption of flip flops to reduce the overall system power consumption. The power specification of modern portable digital circuits is severely limited. It is very essential to improve system power performance in the flip flop networks. Timing elements like flip-flops are very important for the performance of digital systems. This is due to the extremely large set up time and hold time. These are also essential for good performance and better efficiency. Recovery or recycling of energy in a circuit is a technique for low

power digital circuits [5]. Energy recovery circuits can be designed to achieve low energy dissipations. This can be achieved by restricting the current to flow across circuit. As a result there is minimum amount of voltage drop across the circuit components. This type of circuits use pulsed power supply or sinusoidal power supply. In this scope, we have applied energy recovery or adiabatic techniques to the clock network. The basic signal which is used for clock supply is the most vital signal. Generally, the nature of the signal is capacitive. The principle used in energy recovery circuits is that, they recycle the energy from the output load capacitance to the input node. This happens during each operation cycle. The power consumption of the clock networks contributes more than 60% of the total power in high performance high speed VLSI systems [6]. Hence, low power clocking methodologies are essential for ultra low power design. Adiabatic flip-flops can use energy recovery process from the clock network. This results significant reduction of power dissipation. In single phase sinusoidal clock these low power flip-flops can operate. This clock can be generated with very high efficiency and energy recycling elements. We have implemented the clock based flip-flops in cadence digital simulator and obtained the results. In this project, we have discussed and compared two basic types of energy recovery flip flops. They are single ended conditional capturing energy recovery flip- flop (SCCER) and differential conditional capturing energy recovery flip flop (DCCER). We have estimated their power dissipation and timing specification constraints. We have also introduced clock gating technique. For the energy recovery clocked flip flops it is clearly seen that they reduce power consumption and propagation delay of the system.

2. LITERATURE SURVEY

Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST implemented in HDL by R. Vara PrasadaRao, N. Anjaneya Varaprasad, G. Sudhakar Babu, C. Murali Mohan

LFSR based Pseudo random test pattern generator is used in the testing of ASIC chips which generates random sequences of test patterns. This project deals with the design of LFSR and also how to multiplex the Test inputs with the ASIC inputs to reduce the additional test input pins required for the ASIC. This project presents a novel low-transition Linear Feedback Shift Register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS'89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively. Index Terms Built-in self-test (BIST), linear feedback shift register (LFSR), low-power test, pseudorandom pattern generator, scanchain ordering, weighted switching activity (WSA).

Study and analysis of various LFSR architecture by Roshni Oommen, Merin K George, Sharon Joseph

In large scale integration process, lots of transistors are implanted on a single silicon substrate for setting up of intricate circuits. Accordingly, major problem of power dissipation comes into the picture. Linear Feedback Shift Register (LFSR) is a commonly used pseudo random sequence generator to generate random 1s and 0s. It is used in applications such as Built-in-self test (BIST), cryptography etc. LFSR's are having high level of fault coverage so they are used in several coding schemes. In this paper, LFSR is implemented using Complementary Metal Oxide Semiconductor (CMOS), Gate Diffusion Input (GDI), modified GDI(mGDI) and Multi Threshold CMOS (MTCMOS) techniques in Cadence Virtuoso using 180nm technology. Simulations of these circuits are done and different parameters like power, propagation delay and area are compared. mGDI gives a reduction of 30%, 39%, 49% with respect to CMOS in power, delay and area respectively and a reduction of 6%, 14% with respect to GDI in power, and delay respectively. Thus, mGDI LFSR design can be employed for low power testing.

3. EXISTING SYSTEM

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design 1, 2. Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations [3]–[8]. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In [9], a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique [10]–[13]. In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data “1” and “0” the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product(PDP) performances.

4. IMPLEMENTED SYSTEM

In general, LFSR is combination of flip-flop and XOR gate. Our proposed system is a combination of GDI and CDFF techniques

as discussed earlier. XOR gate is implemented using GDI and flip-flop is implemented using conditional discharge technology.

XOR USING GDI

The GDI technique reduces the area and power in the design of VLSI circuits. GDI implements the functions using at most two MOS transistors. The three inputs of a simplest GDI cell: combining the gate input of pMOS and nMOS, the common input is denoted as G, P is the source feed of pMOS, and nMOS source feed is N which is shown in Fig 3. In GDI mass of pMOS and nMOS are connected to P or N terminals instead of connecting to GND and VDD. The objective of GDI are reduction of transistors count, low power dissipation and simple gates. Fig 3 displays the XOR gate implementation using GDI technique. It consists of a body gate and an inverter. One of the input controls body gate and other input is connected to the pMOS transistor bulk whereas the nMOS bulk terminal is connected to output of inverter nMOS. Clock signal fed to body gates determines the state of the circuit. With respect to the preset input initial value of LFSR is set. Lesser dissipation of power, power delay and area achieved through this technique.

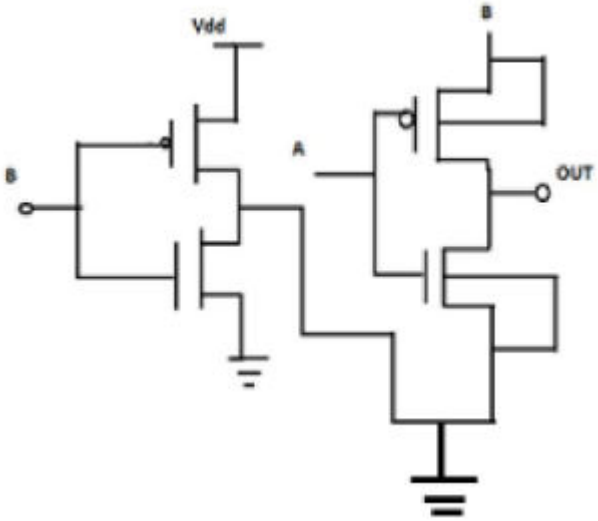

Fig 1: XOR using GDI

PROPOSED CONDITIONAL DISCHARGE TECHNIQUE

The clock-gating in the conditional capture technique results in redundant power consumed by the gate controlling the delivery of the delayed clock to the flip-flop. As a result, conditional precharge technique outperformed the conditional capture technique in reducing the flip-flop EDP [16]. But the conditional precharge technique has been applied only to ip-FF, and it is difficult to use a double-edge triggering mechanism for these flip-flops, as it will require a lot of transistors. A new technique, conditional discharge technique, is proposed in this paper for both implicit and explicit pulse-triggered flip-flops without the problems associated with the conditional capture technique, In this technique, the extra switching activity is eliminated by controlling the discharge

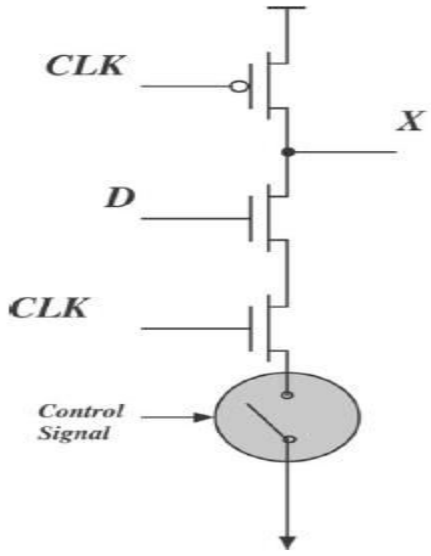

Fig. 2. Proposed conditional discharge technique

Fig. 2. Conditional capture technique. path when the input is stable HIGH and, thus, the name Conditional Discharge Technique. In this scheme, an nMOS transistor controlled by is inserted in the discharge

path of the stage with the high-switching activity. When the input undergoes a LOW-to-HIGH transition, the output changes to HIGH and to LOW. This transition at the output switches off the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable HIGH.

CONDITIONAL DISCHARGE FLIP-FLOP (CDFF)

Conditional discharge flip-flop (CDFF) has two stages, responsibility of LOW-to-HIGH transition is taken by stage one. In the sampling window when input is HIGH, discharging of the internal node is initiated (X), assume Q- LOW, Qb- HIGH for enabling the discharge path. In the second stage the output node will be charged to HIGH as a result.

HIGH-to-LOW input transition is capture in Stage 2. If LOW input is fed at the period of sampling, the disabling of first stage takes place, and pre charge state is continued in intermediate node. As the result, Y node is HIGH and in the sampling period the second stage discharge path gets enabled that allows the output node to discharge and captures the input data. Fig 3, shows the simple implementation of a flip flop

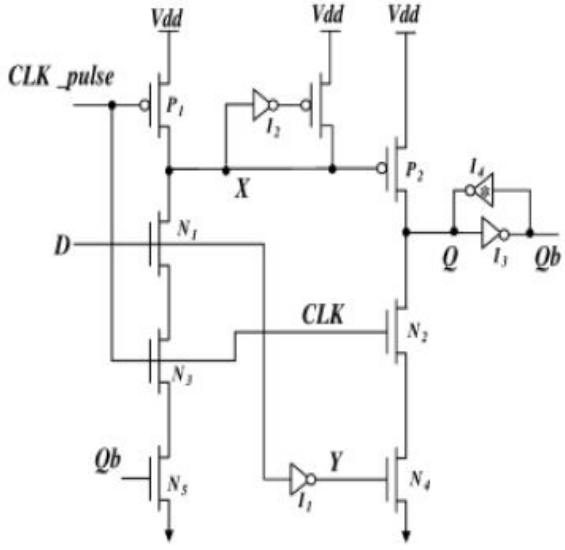

Fig 3: Flip flop using CDFF

The schematic diagram of the proposed flip-flop, conditional discharge flip-flop (CDFF), is shown in Fig. 7. It uses a pulse generator as in [9], which is suitable for double-edge sampling. The flip-flop is made up of two stages. Stage one is responsible for capturing the LOW-to-HIGH transition. If the input is HIGH in the sampling window, the internal node is discharged, assuming that were initially (LOW, HIGH) for the discharge path to be enabled. As a result, the utput node will be charged to HIGH through P2 in the second stage. Stage 2 captures the HIGH-to-LOW input transition. If the input was LOW during the sampling period, then the first stage is disabled, and node retains its precharge state. Whereas, node will be HIGH, and the discharge path in the second stage will be enabled in the sampling period, allowing the output node to discharge and to correctly capture the input data. The conditional discharging scheme is employed in the CDFF as follows: in order to reduce the redundant switch power, we employ a discharge control transistor N5 at the discharge path of the first stage. When , which means and , N5 turns on, and the discharge path is enabled. If the input makes a LOW-to-HIGH transition, and CLK_pulse is HIGH, N1, N5, and N3 switch on, the internal node is discharged to LOW, and is pulled up to HIGH with pulled down to LOW, which shuts off the nMOS stack in first stage. For this transition (LOW-to-HIGH), is discharged only once; i.e., consecutive HIGH level at will not be sampled because the discharging path is inhibited by . To ensure that the HIGH-to-LOW transition is sampled by the flip-flop, dual path is used. Recall that the output rise transition tends to be the slow path (critical path); by employing dual path, capacity at node

is reduced, and thus the LOW-to-HIGH delay could be reduced. Since node is not charged and discharged every clock cycle,

no glitches appear on the output node when the input stays high, and will not be discharged at the beginning of each evaluation [22] as that in the other precharged dynamic circuits such as HLFF, SDFF, or ip-DCO. As a result, CDFF features less switching noise generation, which is an important issue in mixed signal circuits. Moreover, node stays HIGH or precharged in most cases, which helps in simplifying the keeper structure as shown in Fig. 7, and it also reduces the capacitive load at node Double-edge triggered pulse generator [9] is utilized to further reduce power on the clock tree and the clocked transistors in pulse generator. Double-edge triggered flip-flops can have the same data throughput as the single-edge triggered flip-flops. The power saved in the clock distribution network is not included when we compare the power consumption. Also, clockgating [23], [24] can be easily applied to eliminate power consumption when keeps the same value. Although the input load is increased, the overall power saving could be achieved significantly.

5. RESULT

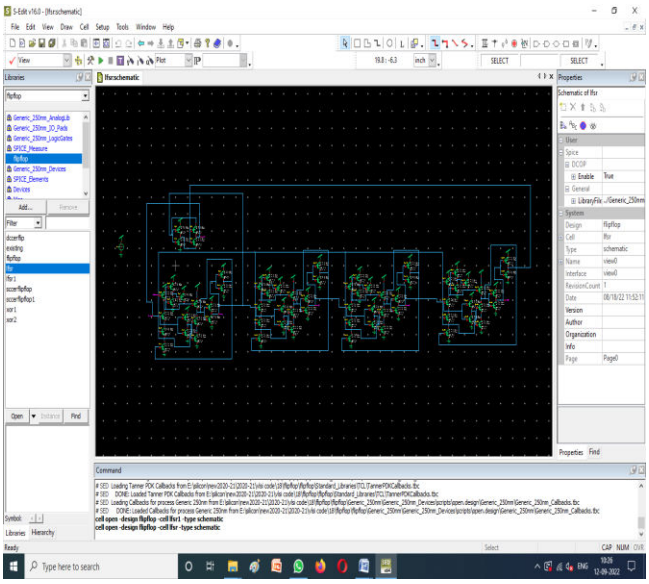

Fig 4: Circuit of lfsr

Fig 5: Simulation result of lfsr

	EXISTING SYSTEM	PROPOSED SYSTEM
TRANSISTOR	72	68
POWER	$2.7174*10^{-2}$	$1.2196*10^{-8}$

Fig 6 Compression Table

6. CONCLUSION

The efficient power consumption of LFSR is achieved through conventional discharge flip flop and gain diffusion input based XOR gate. This proposed model is 33% efficient in power consumption to that of normal LFSR architecture. Using this model the many applications like generation of pseudo random sequences can be achieved with low power consumption architecture.

7. FUTURE SCOPE

We hope that presented results will encourage further research activities in TCFF technique. The issue of sequential logic design with TCFF is currently being explored, as well as technology compatibility. More work was recently done in automation of logic design methodology based on TCFF technology.

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