DESIGN OF LOGICALLY OBFUSCATED N-BIT ALU FOR ENHANCED SECURITY

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ABSTRACT: The New Technology is quantum dot cellular automata was developed at Nanoscale level, which required less area by utilizing quantum cells compared to CMOS technology thus it consumes low power. The CMOS based Transistors can reduce their channel width at only certain levels than their present size .The QCA approach tends to one of the best arrangements in beating this physical width and channel width at molecular level. we can perform any Digital Logic Function, with the avail of QCA based majority gates. In this paper fast adders like Ripple carry adders(RCA) Ripple carry subtractors and Array multipliers of N-bit size operations are performed by utilizing Majority gates that has all best in class contenders and accomplishes the best area-delay tradeoff, delay (speed), power utilization and PDP.

INTRODUCTION

1.1 OVERVIEW

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed).Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user constraints in efficient manner without any violation otherwise, improving performance of the design.

Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Quantum-dot cellular automata (QCA) which employs array of coupled quantum dots to implement Boolean logic function. The advantage of QCA lies in the extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic “0”and “1”.The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay.i.e by calculating the propagation and generational carries.

Quantum dots are semiconductors confined in all three dimensions of space or alternatively, it can be noted that Quantum dot is a simple charge container and it is three dimensionally confined [8]. The promising alternative of CMOS paradigm is the Quantum dot cellular Automata (QCA) which is used to represent the information in binary M’ and binary ‘O’ in terms of electronic charge configuration. In 1993, C. S. Lent et al. first introduced the theoretical Quantum dot Cellular Automata [3] and in early 1999, C. S. Lent et al. described the experimental approach to design QCA cell with GaAs [8]. The dynamic behaviour of QCA was discussed with the help ofthe hart tree approximation [4], Quantum mechanics is also involved in finding out the cell size and dot radius of a single QCA cell. Hence, QCA became research interest to establish as strong CMOS alternative. During last decades, in nanotechnology era, an exhaustive research has been carried out in this domain. QCA is still in infancy stage, needs lots ofstudy for QCA logic circuit design. The low

power reversible logic circuit design, tile based logic circuit design as well as its defect analysis are prime problem domain. The ternary computing with QCA is most challenging task in this domain since no such improvement is noticed. The multivalued computing, specifically ternary computing is an emerging domain of research due the potential advantages like greater data storage capability, faster arithmetic operations, better support for numerical analysis, application ofnon-deterministic and heuristic procedures, communication protocol and effective solution for non-binary problems. Nano-scale logic circuit fabrication is suffering from defects that may occur during fabrication. It is also noticed that QCA fabrication is suffering from high probability of defect. It was reported in several proposals [59-60, 63-70] that defects are considered mainly on deposition phase. It is assumed that successful chemically synthesized QCA cells are deposited on the substrate. In this phase three common defects that had been analyzed are (a) extra cell deposition i.e. extra QCA cell/s is/are deposited than the original requirement of cell arrangement, (b) missing cell deposition/ un-deposited cell deposition, i.e. the QCA cell/s is/are not deposited as required in original design, (c) displaced /misplaced cell deposition, i.e. QCA cell/s is/are misplaced from the exact position of deposition. These three types of defects may cause major 2 fatal errors in QCA manufacturing. The device or gate design using QCA required a permissible defect tolerance on the above-mentioned defects such that the device no longer loses its characteristics. Hence, defect analysis is becoming most promising problem domain in QCA

1.2 PROBLEM STATEMENT

It is well known that the Complementary Metal Oxide Semiconductor (CMOS) technology based digital computers conceived two innovative ideas, in one idea information are represented with binary ‘O’ and binary ‘ 1 ’ and another one is that electronic charge state is used to represent the information in terms of current switch. The CMOS provides micro scale computing with high density and low power Large Scale Integrated Circuit (VLSI), However, such technology was found to have several drawbacks like high leakage of current, power dissipation in terms of heat, and limitation of speed in GHz range. Moreover, this technology has arrived at its limitation as per Moore’s Law, i.e., unit cost is shrinking as number of circuit components rises. Every eighteen months number of circuit components become double [1] as well as the industry is now facing an increasing important trends of “More-than-Moore”, reported in the Semiconductor Industries Association’s International Roadmap for Semiconductors [2]. Researchers have to find out a strong alternative of CMOS technology for VLSI design. Nanotechnology was found as a strong alternative, subject to some confusion and controversy and complicated by the fact that there are naturally occurring nano size materials and other nanosize particle, in the range from 1pm down to 10A. Nanotechnologies won its existence in development within field ofmicroelectronics. Nanomechanical computing elements are scalable in terms ofinput size and depth ofpropagation path analyzed using a bounded continuum model. Boolean logic functions ofNOT, AND, OR, and XOR are realized. Nanotechnology should not be viewed as a single technology that only affects the specific area. It compensates the limitation in many existing technology. Quantum dot Cellular Automaton (QCA) is an emerging research domain in nanotechnology [3-10].

1.3 MOTIVATION

Quantum Dot Cellular Automata (sometimes referred to simply as quantum cellular automata, or QCA) are proposed models of quantum computation, which have been devised in analogy to conventional models of cellular automata introduced by von Neumann. Standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Just like any CA, Quantum (-dot) Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them.

II.ESSENTIALS OF QUANTUM-DOT CELLULAR AUTOMATA

2.1 Introduction

This chapter will provide the background material needed for a full and complete discussion of the work to be presented in this thesis. The chapter begins with a discussion of the QCA device and then extends to logical circuits that are constructed from the basic QCA device. The chapter includes the discussion on how QCA devices are clocked. Then the chapter concludes with the different models of the QCA.

2.2 QCA Device Background

QCA cells perform computation by interacting coulombically with neighboring cells to influence each other's polarization. In the following subsections we review some simple, yet essential, QCA logical devices: a majority gate, QCA wires, and more complex combinations of QCA cells.

2.2.1 The Basic QCA Device

The basic device in QCA is a QCA cell which enables both the computation and transmission of the information. A QCA cell consists of a hypothetical square space with four electronic sites and two electrons. The electronics sites, called Dots, represent the locations which the electrons can occupy. The dots are coupled through quantum mechanical tunneling barriers and electrons can tunnel through them depending on the state of the system. Exactly two mobile electrons are loaded in the cell and can move to different quantum dots in the QCA cell by means of electron tunneling. Tunneling paths are represented by the lines connecting the quantum dots in Figure 2.1. Coulombic repulsion will cause the electrons to occupy only the corners of the QCA cell resulting in two specific polarizations [122]. Electron tunneling is assumed to be completely controllable by potential barriers (that would exist underneath the cell) that can be raised and lowered between adjacent QCA cells by means of capacitive plates.

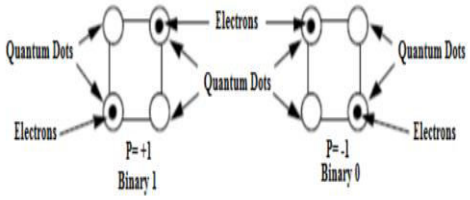


Figure 2.1. QCA cell polarizations and representations of binary 1 and binary 0.

For an isolated cell there are two energetically minimal equivalent arrangements of the two electrons in the QCA cell, denoted cell polarization P = +1 and cell polarization P = -1. Cell polarization P = +1 represents a binary 1 while cell polarization P = -1 represents a binary 0. This concept is also illustrated graphically in Figure 2.1. It is also worth noting that there is an unpolarized state as well. In an unpolarized state, inter-dot potential barriers are lowered which reduces the confinement of the electrons on the individual quantum dots. Consequently, the cells exhibit little or no polarization and the twoelectron wave functions have delocalized across the cell [133] as shown in Figure 2.2

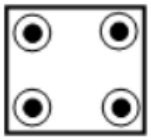


Figure 2.2. QCA unpolarized cell.

The numbering of dots denoted by i in the cell goes clockwise starting from the dot on the top right with i =1, bottom right dot i =2, bottom left dot i =3, and top left dot i=4. The polarization P in a cell is defined as Where Pi denotes the electronic charge at dot i. The polarization measures the charge configuration i.e. the extent to which the electronic charge is distributed among the four dots [3] [90].

2.2.2 Cell-to-Cell Response

Figure 2.3 illustrates the cell-to-cell response function, in which the polarization P2 of cell 2 is induced by the fixed polarization of a driver (i.e., its neighbor, or cell 1 in this case) [90]. In the ground state of this two-cell system (that corresponds to a correct computation), the polarization P2 is aligned with its neighbor polarization P1. The cell-cell response curve can be computed by solving the two particle Schrodinger equation [122]. It can be seen that the cell-cell response is highly non-linear, which indicates signal restoration. Even a slightly polarized input cell induces an almost fully polarized output cell.

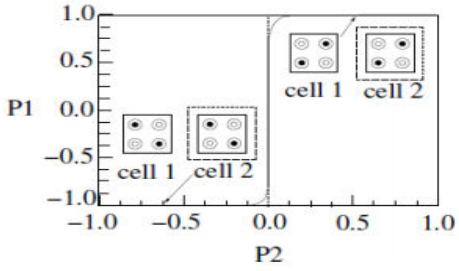


Figure 2.3. Non-linear cell to cell response function.

A driver of a QCA cell could be an input device such as a nanotube, a very thin wire or a tip of a scanning tunneling microscope (STM). In semiconductor QCA, a standard technique called “plunger electrode” has been used to alter the electron occupancy of the input cell [123] [124] [125]. Reading the output state of a QCA cell is difficult, because the required measurement process must not change the charge of the output cell. Electrometers made from ballistic point-contacts [126] [127], the STM method [128], and SET electrometer have been used to read the output. Unlike conventional logic circuits in which information is transferred

by electrical current, QCA operates by the Coulombic interaction that connects the state of one cell to the state of its neighbors.

2.2.3 Majority Logic Gate

The fundamental QCA logical circuit is the three-input majority logic gate [3] that appears in Figure 2.4 from which more complex circuits can be built. The basic majority gate is obtained by placing four neighboring cells adjoining to a device cell, which is in the middle. Three of the side cells are used as inputs, while the remaining one is the output. The device cell will always assume the majority polarization because it is this polarization where electron repulsion between the electrons in the three input cells and the device cell will be at a minimum.

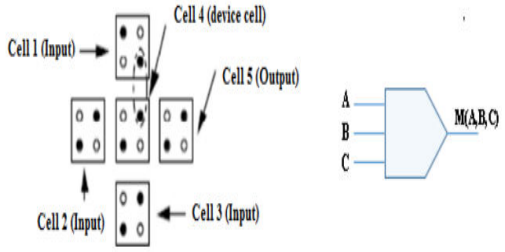


Figure 2.4. The fundamental QCA logical device - the majority gate

To understand how the device cell reaches its lowest energy state (and hence P= +1 in Figure 2.2), consider the Coulombic interaction between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Coulombic interaction between electrons in cells 1 and 4 would normally result in cell 4 changing its polarization because of electron repulsion (assuming cell 1 is an input cell). However, cells 2 and 3 also influence the polarization of cell 4 and have polarization P=+1. Consequently, because the majority of the cells influencing the device cell have polarization 1+ =P , it too will also assume this polarization because the forces of Coulombic interaction are stronger for it than for 1. The equation of majority logic gate can be realized as:– =P AC+ BC + AB=F The truth table of the majority logic gate is given in Table 2.1.

Inputs		Output	
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 2.1: Truth table of majority logic gate

III.LITERATURE SURVEY

The evolution of electronic information technology (IT) and communications has been mainly possible by continuous progress in silicon-based Complementary Metal Oxide Semiconductor (CMOS) technology. This continuous progress has been maintained mostly by its dimensional scaling, which results in exponential growth in both device density and performance. The reduction in costperfunction has steadily been increasing the economic productivity with every new technology. In addition to its scalability, the unique device properties such as high input resistance, self - isolation, zero static power dissipation, simple layout and process steps have made CMOS transistors as the main components of CMOS integrated circuits (ICs). However,the dimensions of CMOS transistor shrinks and approaches towards the close proximity between source and drain, which reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region. Thus avoiding further reduction size.

Dimensional scaling of CMOS transistors is reaching their fundamental physical limits [24-25]. Therefore, research has been actively carried out to find an alternative way to continue to follow Moore's law. Among these efforts, various kinds of alternative memory and logic devices, so called "Beyond CMOS Devices," have been proposed [8]. These nano-devices take advantage of the quantum mechanical phenomena and ballistic transport characteristics under lower supply voltage and hence low power consumption. These devices are expected to be used for ultra-high density integrated electronic computers due to their extremely small size.

Nano-wire Field-Effect Transistors (NWFETs) have drawn promising attention and have been considered an alternative to continue CMOS scaling, since their nonplanar geometry provides

superior electrostatic control of the channel than the conventional counter parts. The increasing attention in Nano-wire research stems from several key factors; their cost-effective "bottom–up" fabrication and high-yield reproducible electronic properties [26-28], which pave way for some fabrication challenges, higher carrier mobility, smooth surfaces and the ability to produce radial and axial Nano-wire hetero-structures [29-30], better scalability resulting from the fact that diameter of Nano-wires can be controlled down to well below 10 nm [31-32]. However, due to their smaller diameters, the inversion charge changes from surface inversion to bulk inversion due to quantum confinement. Thus, variations in Nano-wire dimensions due to fabrication imperfections can lead to perturbations in the carrier potential and scattering that degrade the charge transport characteristics. Also, variations in Nano-wire diameters may lead to a variation in FET threshold voltage. Reducing variability is therefore a key challenge in making Nano-wire FETs a viable technology. Furthermore, quantum confinement effects make modeling of Nano-wire transistors a complex problem. The physics related to the operation of Nano-wire transistors needs to be well articulated so that simple compact models, including ballistic transport and realistic sub band parameters, can be developed for circuit design using SPICE-like simulators [33].

IV.EXISTING ARCHITECHURE

The ALU operations are primarily divided into Arithmetic operations and Logical operations. The Arithmetic operations like Addition, Subtraction, Increment, Decrement and so on are performed by Arithmetic unit, while Logical unit performs AND, OR, XOR, complement, rotate, shift operations etc. The multiplexers and de-multiplexers play a vital role in selecting the respective results generated by the ALU. The Microcontrollers need to handle the individual port lines which necessitate the need for bit handling instructions. Thus, an ALU of a Microcontroller needs to cater to both the bitwise and the byte-wise Logical operations, arithmetic and data transfer operations. In spite of incorporating all the ALU operations, the challenges lie in optimizing the area occupied on the chip.

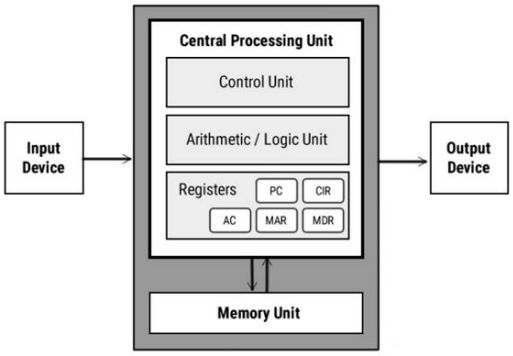


Fig. 4.1. A typical depiction of proposed ALU architecture

The basic circuit for the design of an arithmetic unit is a full adder. There are multiple ways in which various types of adders are designed like Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSeA) etc. The respective adders are selected based on the parameter to be minimized. If the focus is on reducing the delay, then CSeA would be a better choice but penalizes with a large chip area and more power-hungry. While CLA would be relatively slower than the CSeA but occupies significantly lesser area. The CSA would be a better choice as the number of bits needed to be added increases as in case of multipliers. The RCA occupies the least possible area but is slower as the number of bits to be added increases.

The proposed architecture focuses on the area optimization and hence RCA has been used in the entire design. The ALU is designed to be incorporated in a Microcontroller along with a barrel shifter to make logical operation yield quicker results. Since the clock frequency targeted for the microcontroller is 20MHz, the speed of operation has not been considered. The complete instruction set of the ALU has been designed.

IV.PROPOSED ARCHITECTURE

5. 1. INTRODUCTION

There are two vigorously irrelevant approaches of two electrons in the QCA cell for an evacuated cell, expected cell polarization P=+1 and cell polarization P=-1, while Cell polarization P=+1 alludes to parallel 1 while cell polarization P=-1 alludes to relating 0. In expansion, this thought is graphically portrayed in figure - 1. It is additionally colossal that there is an unpolarized state as well. In an unpolarized

state, potential points of confinement between contact are diminished which diminishes the exhibit generally zero polarization and the two electron wave limits have been delocalized over the telephones appeared in Figure 1

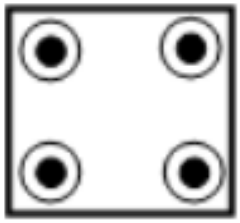


Fig 5.1. Unpolarized cell

The numbering of specks signified by electrons in the cell goes clockwise beginning from the matrix on the upper appropriate with quantum level I =1, base right cell-I =2, base left cell I =3, and upper left cell i=4. The polarization level P in a cell is characterized as Where Pi means the electronic charge at speck current. The polarization estimates the charge design for example the degree to which the electronic charge is appropriated among the four cells. The basic QCA sensible circuit is the three-input majority gate (MG) that shows up in Figure 2 from which progressively complex circuits can be fabricated. The fundamental MG gates are acquired by setting four neighboring cells bordering to a quantum cell, which is in the center. Three of the side cells are utilized as data sources, while the staying one is the yield. The quantum cell will consistently expect the majority polarization is where there will be at least charge between the electrons in the three information cells and the quantum cell.

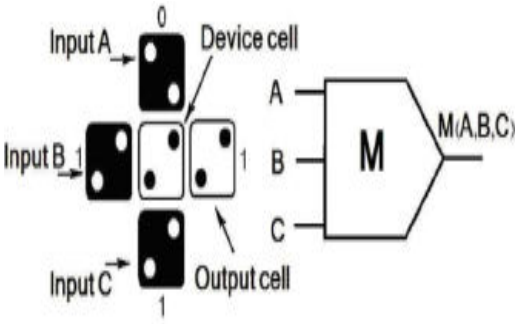


Fig 5.2. Majority gate using QCA

Consider the coulombic interface between cells 1 and 4,cells 2 and 4,cells 3 and 4 to perceive how the contraption cell accomplishes its most minimal imperativeness state (and from now on P=+1 in figure2).Typically, coulombic association between electrons in cells 1and 4 would make 4 change its polarization in light of electron stun. (expecting cell 1 is a data cell). In any case, cells 2 and 3 in like manner sway the polarization of cell 4 and have polarization P=+1. Along these lines, in light of the way that the greater part of the cells influencing the contraption cell have polarization 1 P , it additionally will moreover expect this polarization because the forces of Coulombic association are more grounded for it than for 1.

5.2. BASIC DESIGN

In current years, a variety of structures have acquainted with improve the productivity of the Nano calculator. In any case, there are just a couple of structures that have been proposed for QCA based Nano-calculator [1] incorporate adders, multiplexer with the detail of their plans. In addition, QCA Adder is a significant block in the caluclation units since multiplication and subtraction tasks can be helped out through the progressive sum activity and two's supplement, separately. Different structures have displayed for QCA adder, which characterized into the single layer [2]–[4] and numerous layer plans. The current multiplexers can be arranged into the single layer [5]–[7] and multilayer circuits. Lamentably, the greater part of the existing methods of the Nano-calculator structures have not clear the important data about their plans, for example, the quantity of quantum cells, No. of MG gates, area and power consumption.

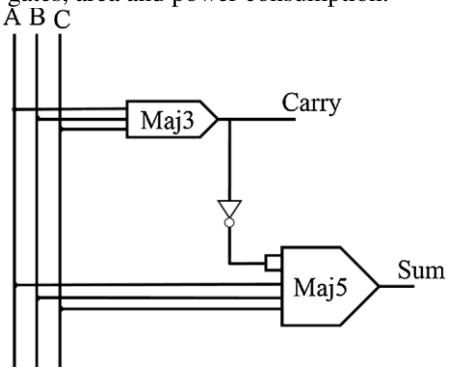


Fig 5.3. Schematic of Existing 1-bit Full adder

The Figure 3 represents the 1 bit full adder operation, which is implemented by using majority gates of 3 input and 5 input which is considered from literature [2]. To design the full adder they used the following equations

$$C_o = M_3(A, B, C_{in})$$

$$S = M_5(A, B, C_{in}, C_o', C_o')$$

A full subtractor is utilized to plays out the subtraction opeartion of three inputs A,B and C. The two yields of subtractor circuit are difference 'D' and borrow 'B'. To execute full

subtractor in QCA it required the inverters as far as MGs, which can be given by

$$B_o = M_3(A', B, C)$$

$$D = M_5'(A', B, C, B_o', B_o')$$

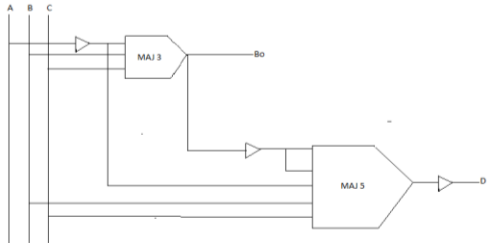


Fig. 5.4. Schematic of Existing Full Subtractor design

The schematic depiction of full subtractor circuit is appeared by Fig.4. The utilization of 5-input MGs make the circuit more straightforward than utilizing just 3-input MG and inverter from literature [2].

5.3. PROPOSED DESIGN:

The major drawback from the above literature is that they consumed the more area, thus they used the more power consumption. The number of majority gates they used to generate the full adder and subtractions are two 3-input Majority gates, two 5-input majority gates And also they required the four inverter gates. To optimize this the new design has been developed which is works both full adder and full subtractor at a time.

5.3.1 PROPOSED ADDERS AND SUBTRACTORS:

The proposed method is implemented with only three 3-input majority gates and two inverters and there is no need of five input majority gates. So the number of quantum cells will reduced in this design method, it causes to reduce the area as well as power.

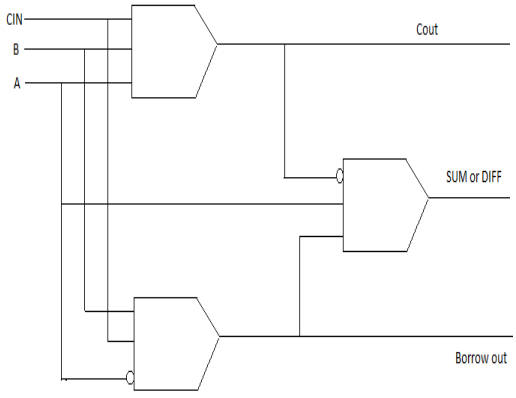


Fig. 5.5. Schematic of proposed Full adder and Subtractor

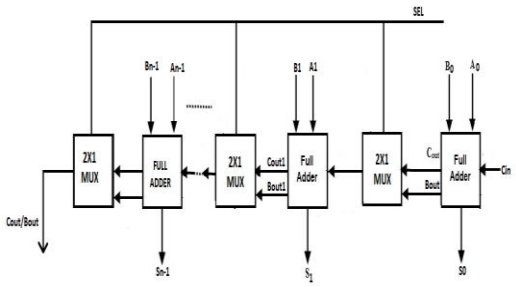


Fig. 5.6. Schematic of proposed N-bit adder and Subtractor

The above figure represents the Full adder and Subtractor, here the single circuit will performs the both operations. Majority gate M1 will generate the carry out and Majority gate M2 will generate the borrow out. Carry out and Borrow out as well as input A will be applied as inputs to the 3rd majority gate to generate the sum or diff.

The above figure represent the N-bit adder and Subtractor by connecting the series manner of N stages. The each FAFS block represents the fig 5 with the majority logics. Here, the carry out and borrow out of the first FAFS block will be applied as input to the next stage. If we required adder as the functionality then carry out will be applied as carry in by making the selection line of 2to1mux to zero, If we required subtractor as the functionality then borrow out will be applied as carry in by making the selection line of 2to1mux to one. The mux operation using majority gates will be explained in this paper in further chapters.

5.3.2 PROPOSED MULTIPLIERS

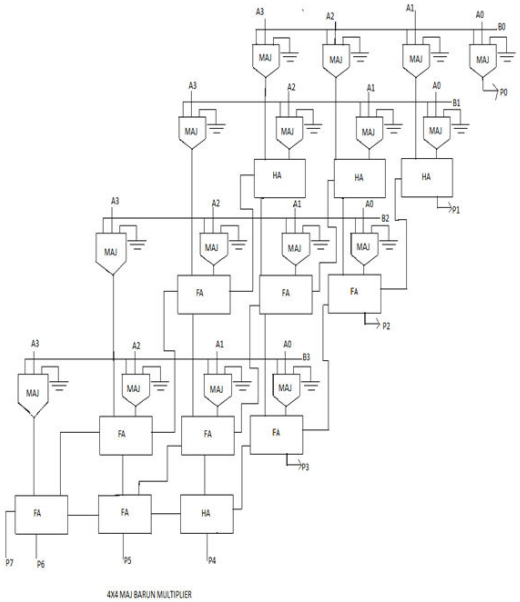


Fig. 5.7. Schematic of 4x4 Barun Multiplier

The above figure performs the 4 bit multiplication operation between A,B. Initially, 16 partial precuts namely A0B0, A1B0, A0B1 and so on generated by using bitwise Majority gates operation between A,B and ground. By making any one of the input zero in the majority gate it will act as the AND gate. For implementing the half adder, by making the anyone of the input in Full-adder zero and the Full adder circuit is represented in Fig 5.

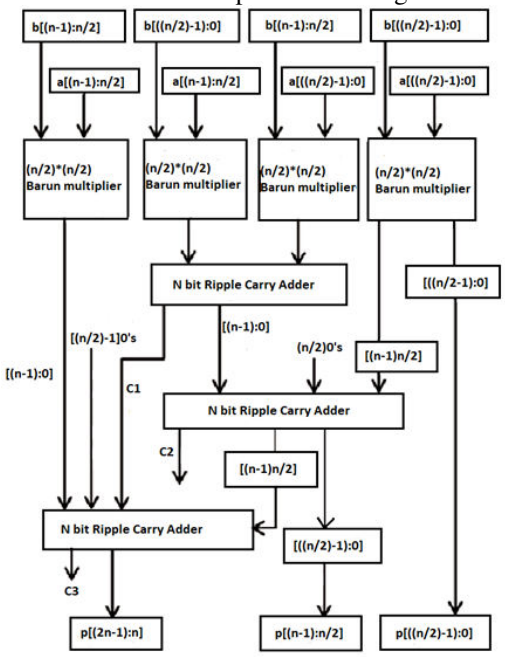


Figure 5.8 : Schematic diagram of N bit multiplier

For develop the N-bit multiplier, it needs 4 Nby2 multipliers. For example, for implementing 8 bit multiplier it requires four 4-bit baurn multipliers. Here, three N-bit Ripple carry adders are used as developed in fig. 6 in this paper. First adder adds the outputs of second and third multiplier partial products here, and addition output will forward to second stage adder. First Nby2 baurn multiplier half of the lsb output bits fed as the final outputs, next half msb output bits fed as the input to the second stage adder. in order to avoid the size of array mismatches Nby2 zeros added to second and third stage adders. After completing the all successful addition product P will generate.

5.3.3 LOGICAL UNIT

As part of the logical unit here we are considered either AND operations and OR operations. By making anyone of input zero in majority gate it will act as the AND gate and similarly by making anyone of input or in majority gate it will act as the OR gate. Inversions of AND, OR gate will create the universal gates like NAND and NOR gates. In the, The FAFS deisgn it has SD pin as three input XOR function, and inversion of it creates XNOR gate.

5.3.4 PROPOSED 4to1 MULTIPLEXER:

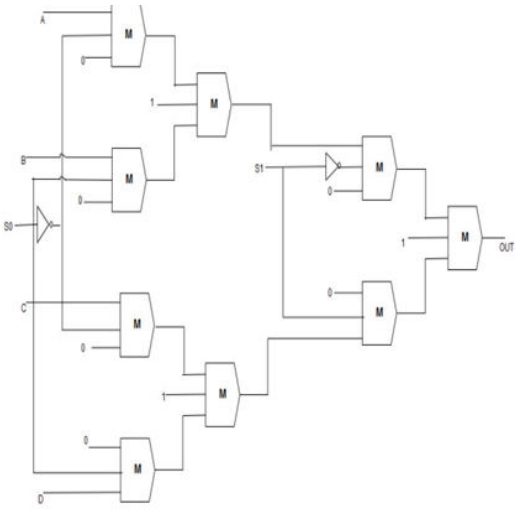


Figure 5.9: 4to1 multiplexer using QCA

A 4to1 Multiplexer can be implemented with by the series and parallel design of 2:1 multiplexer. The equation of 4:1 multiplexer can be derived as:

F=D.S0.S1+C.S0.S1B+ B.S0B.S1+ A.S0B.S1B.

Where S0, S1 represents the selection lines and A, B, C, D represents the 4to1 multiplexer inputs, S1B, SOB are compliments of S1 and S0. The MG gate representation of the 4:1 multiplexer is shown in Figure 9.

5.3.5 ALU:

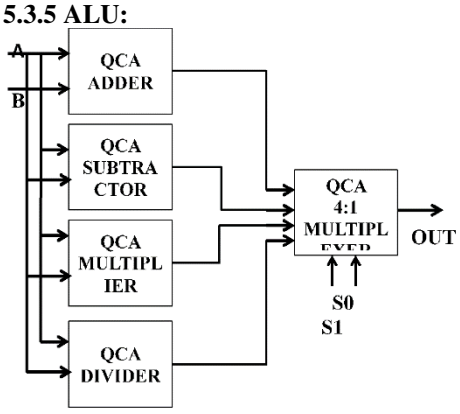
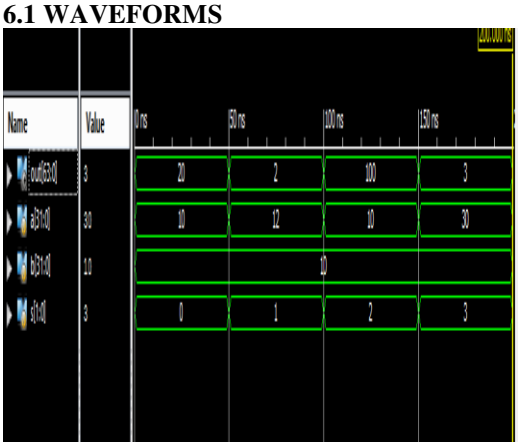


Figure5.10: Block diagram of Nano-Caluculator

The proposed Nano-Caluculator performs four operations between inputs A and B. when multiplexer selection lines S0 and S1 becomes {0, 0}, it will functions as Adder, similarly for {0,1}functions as subtractor, for {1,0} functions as multiplier and for {1,1} act as logical unit.

VI.SIMULATION RESULTS

6.1 WAVEFORMS



The above result represents the simulation waveform by using the Xilinx ISE software. Where S is the selection line, if s is 0 then a,b {10,10}added generates the output as 20, s is 1 then a,b {12,10}subtracted generates the output as 2, s is 2 then a,b {10,10}multiplied generates the output as 100 and s is 3 then a,b {30,10}logical unit generates the result as 3.

6.2 DESIGN SUMMARY

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	4982	204000	2%
Number of fully used LUT-FF pairs	0	4982	0%
Number of bonded IOBs	131	600	21%

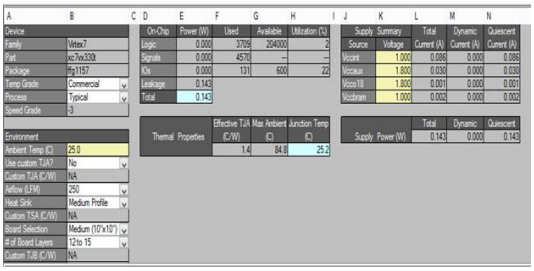
The above result represents the synthesis implementation by using the Xilinx ISE software. From the above table, it is observed that only 4982 look up tables are used out of available204000. It indicates very less area(2%) was used for the proposed design.

6.3 TIME SUMMARY

```
LUT2:I0->O            1    0.043   0.000  div1/Madd_GND_49_o_GND_49_o_a
MUXCY:S->O            1    0.230   0.000  div1/Madd_GND_49_o_GND_49_o_a
XORCY:CI->O           2    0.251   0.347  div1/Madd_GND_49_o_GND_49_o_a
LUT4:I2->O            1    0.043   0.000  div1/Msub_n0258_Madd_lut<30>
MUXCY:S->O            0    0.230   0.000  div1/Msub_n0258_Madd_cy<30> (
XORCY:CI->O           1    0.251   0.289  div1/Msub_n0258_Madd_xor<31>
LUT5:I4->O            1    0.043   0.279  Mmux_out110 (out_0_OBUF)
OBUF:I->O                 0.000          out_0_OBUF (out<0>)
----------------------------------------
Total                    54.238ns (31.895ns logic, 22.343ns route)
                                  (58.8% logic, 41.2% route)
```

The above result represents the time consumed such as path delays by using the Xilinx ISE software.the consumed path delay is 54.238ns.

6.4 POWER SUMMARY



The above result represents the power consumed by using the Xilinx ISE software. The consumed power is 0.143uw.

COMPARASION TABLE

parameter	EXISTING METHOD[1]	PROPOSED METHOD
Time delay	59.110 ns	54.238 ns
Power utilized	1.293uw	0.143 uw
Look up tables	5277	4982

VII.CONCLUSION

In this paper, a new QCA based N-bit adders, subtractions and multipliers designs has developed to perform the arithmetic and logical operations. The simulation outcome confirms the proposed operations have developed with less cells, area and latency. In addition, to decrease the complication of the addition associated operations, an proficient adder-subtractor has been proposed.

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