IMPLEMENTATION OF THREE-STAGE COMPARATOR AND ITS MODIFIED VERSION WITH HIGH SPEED CONVERSION

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Abstract: The comparator is an essential component in many different kinds of analog-to-digital converters (ADCs). This same comparator speed, kickback noise, input referenced noise, and offset all restrict the ADC sampling rate and accuracy, especially in high-speed, high-resolution SAR ADCs. In this case, an elevated comparator is essential. An improved three-stage comparator and a modified version are shown in this project. The three-stage comparator throughout this study contains an additional amplification step, which enhances the voltage gain and speeds up the process compared to standard two-stage comparators. With the three-stage comparator, nMOS input pairs may be utilized for amplification as well as regeneration in the very same stage, resulting in a significant increase in the comparator's speed. A CMOS input pair is used in the amplification step of the proposed three-stage comparator, it is a modification. Kickback noise is considerably reduced since the nMOS kickback is cancelled out by the pMOS kickback. Inside the regeneration step, it also provides an additional signal route that aids in increasing speed even more. The two-stage and three-stage comparators were built as well as 180-nm CMOS technology for simple comparison. There was a 10x improvement in speed and a 10x reduction in kickback noise using a redesigned three-stage comparator. Although this improvement is welcome, it does not come at the expense of reduced input accuracy or noise.

1.INTRODUCTION

Throughout most analog-to-digital converters, COMPARATOR is indeed an essential building component (ADCs). Fast, low-power comparators are often required by high-speed analog-to-digital converters (ADCs), particularly flash ADCs. Low supply supply voltages are a problem for UDSM CMOS technologies because threshold voltages of something like the devices has be lowered to match the supply voltages of current CMOS processes [1]. Because when supply power gets lowered, it becomes more hard to formulate high-speed comparators. The larger transistors required to offer high speed in a given technology, as well as the increased die area and power, are essential to make up for the decrease in supply voltage. Some high-speed ADC architectures, like flash ADCs, are severely confined in their input range while operating at low voltage as a result. Low-voltage design difficulties have been addressed by techniques including supply boosting, current mode design, and dual-oxide technologies that really can withstand higher supply voltages. Boosting and bootstrapping are 2 methods for addressing input-range and switching issues that rely on increasing the supply, reference, or clock voltage. If you're working with UDSM CMOS technology, you'll have to worry about dependability difficulties. Blalock's body-driven MOSFET approach eliminates the need for a threshold voltage, allowing it to function as a depletion-type device. This method yielded a modulator-specific 1-bit quantizer, which is detailed in the publication. Body-driven transistors possess lower transconductance (equal to gmb of the transistor) then their gate-driven cousins, and specific manufacturing procedures like For make NMOS or PMOS transistors work throughout this body-driven design, you'll need a deep n-well. nMOS and pMOS are

the two types Avoid stacking too many transistors across power supply during low-voltage operation by using novel circuit designs. There will also be technological adjustments. With the typical dynamic comparator, extra circuitry has been added to increase comparator speed at low supply voltages. Using a 0.5 V supply, this comparator's maximal clock frequency is 600 MHz, and its current consumption is 18 nA. Contrary to this method, component mismatches might have a negative influence on such a comparator's performance. Double dynamics comparator early designs seem to have been predicated on something like a separate or cross-coupled stage for the input stage. Fast operation across a large common-mode & supplying voltage range might well be done from any of this isolation.

2. LITERATURE SURVEY

A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise by H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta

A 65-nm CMOS technology implements a latch-type comparator with such a dynamic bias pre-amplifier. To minimise power consumption, main output nodes of the preamplifier are only partly drained when using dynamic bias with such a tail capacitor. The energy usage and input referred noise voltage of both the comparator are studied and compared to those of the previous art. This preamplifier is optimised for minimal noise and high gain using first-order equations. Prior art & dynamic bias are also both implemented on such a single device, and experiments indicate that dynamic bias may cut average energy consumption by around a factor of 2.5 for much the same noise under half supply voltage.

An 8-bit 150-MHz CMOS A/D converter by Y. T. Wang *et al.*,

An 8-bit, 5-stage, pipelined, & interleaved digital-to-analog converter with either an interleaved & interleaved digital-to-analog converter combines differential pairs without source followers as the only analogue process. Sliding interpolation may be used to reduce the need for a large number of comparators or interstage digital-to-analog converters using residual amplifiers. The pipelining approach employs scattered samples over stages to ease the linearity-to-speed tradeoffs using sample-and-hold circuits. Interleaved systems may benefit from a clock edge reassignment methodology that eliminates timing inconsistencies, and a holed interpolation method that decreases integral nonlinearity errors through little speed or power loss is also shown. At 150 MHz, it has a signal-to-noise+distortion ratio of 43.7 dB, with the both differential and integral nonlinearities of 0.62 LSB. all because to its use of CMOS technology with 0.6-/spl mu/m. An area about 1.2/spl times/1.5/sup 2/ mm/sup 2 is required to power the circuit.

Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator by S. Babayan-Mashhadi and R. Lotfi

It is becoming more important to employ dynamic regenerative comparators that enhance speed and power economy in the design of analog-to-digital converters. Analytical expressions with results of a study on dynamic comparators' delay would be provided in this article. Using the analytical formulas, designers may have a better understanding of the major causes of comparator delay as well as completely investigate the tradeoffs within dynamic comparator design. Analyzed circuits have led to the development of an entirely new dynamic comparator that can operate at low power and speed even at low supply voltages, even with a standard double-tail comparator circuit. In order to shorten the delay time, overall design is simplified and

just a few transistors are added to reinforce the good comments during regeneration. The findings of the research are corroborated by post-layout simulations in 0.18-m CMOS. The suggested dynamic comparator is proven to drastically decrease both power usage and delay time. Inside the suggested comparator, the maximum clock frequency may be raised to 2.5 & 1.1 GHz at supply voltages of 1.2 & 0.6 V with a power consumption of 1.42 and 1.43 milliwatts, respectively. At 1.2 V supply, this input-referred offset has standard variation of 7.8 mV.

A Low-Power High-Speed Comparator for Precise Applications by A. Khorami and M. Sharifkhani

Low-power comparators are shown. Both the comparator's preamplifier input and the latch stage employ pMOS transistors. An local clock generator is used to regulate both stages. Latch activation is delayed during the assessment phase in order to obtain adequate preamplification gain and prevent excessive power consumption. As a result of the increased preamplifier gain and decreased latch input common mode due to tiny cross-coupled transistors, the power MOS transistors (at latch input) are turned on more powerfully, resulting in a shorter delay. While traditional comparators use more power, our new design allows us to tailor the delay for preamplification while using less energy. Solid analytical derivations, process–VDD–temperature corners & Monte Carlo simulations were used to demonstrate the comparator's speed advantages and power savings. At the very same offset and practically same noise budget, measurements show a 50% reduction in power consumption as well as a 30% improvement in comparison speed thanks to the circuit under consideration. In addition, the comparator have a rail-to-rail input Vcm range of 500 MHz in fclk=1.

A Low-Power High-Precision Comparator With Time-Domain Bulk-Tuned Offset Cancellation by J. Lu and J. Holleman

A low-power, high-precision dynamic comparator was given a unique time-domain bulk-tuned offset cancellation approach in order to lower its input-referred offset with the least amount of extra power and delay possible. A commercially accessible 0.5-m technique was used to produce the design. Results from 10 circuits demonstrate that the offset standard deviation has been reduced from 5.415 mV to 50.57 V, an improvement of a factor of 107.1. With a broad range of common mode input, this offset cancellation approach can provide quick and robust convergence with no perceptible offset or noise. This comparator and indeed the OC circuits utilise 4.65 W of power, or 23 pJ of energy per comparison, with such a supply voltage of 5 V and a clock frequency of 200 kHz.

3. EXISTING METHOD

Comparator with two stages. Resetting, amplifying, and regenerating are indeed the three stages of the operating cycle. The comparator gets reset during the reset phase (CLK = 0). This input signal VIP–VIN was amplified & delivered to both the latch stage during the amplification phase (CLK = 1). OUTP & OUTN regenerate to VDD or GND during the regeneration phase. Inside the latch stage, its pMOS inputs are limited to a pair, as previously stated.

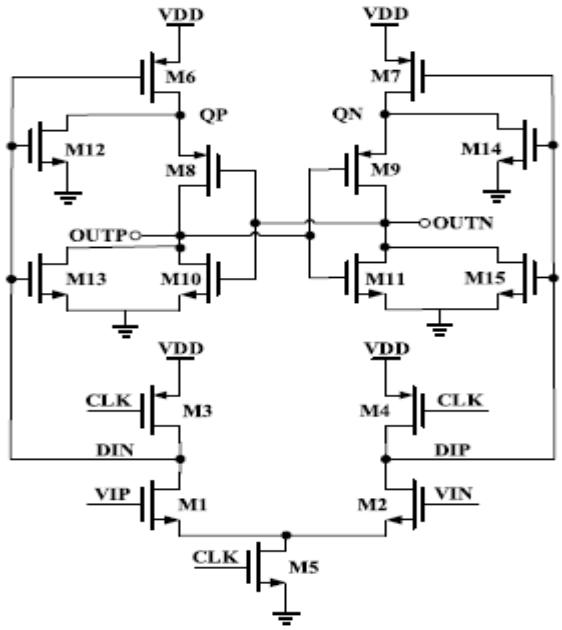

Fig 1 Two-stage comparator

Comparator (M1-15), compensation current source (MC1-2), and circulating current circuit are all part of the circuit.

At reset (CLK = 0), all Di nodes are pre-charged to provide voltage VDD by M3 and M4. This causes the output nodes of M8 & M9 to be discharged to ground. M3 and M4 are turned off, while M5 is activated, during the reset phase. With time, overall common mode voltage declines at the Di nodes, as well as an insight differential voltage would build up mostly in brief time it takes for IM5/CDi (CDi is the load capacitance of the 1st stage) to drop. So because second latch stage must detect VDi at a rather short period td, the typical comparator needs high-accuracy timing CLK.

Di nodes' falling edges may be used to latch the second stage of this suggested comparator. The Di nodes are linked to the M14 and M15 gates rather than M12. Pre-charging switches M14 and M15 additionally serve as input transistors for the second latch stage. As a result, boosting the gain of both the second latch stage improves the comparator's sensitivity. Furthermore, the suggested comparator just requires a single phase clock, easing the clock driving needs. The Xi nodes are reset using M12 and M13 to eliminate comparator offset caused by voltage difference between both the Xi nodes.

These concerns are not present in two-stage comparators. Let's look at an example from [9]: the Miyahara two-stage comparator (see Fig. 4.1). These have no longer been bound by a small current source through its regeneration process. Latch inputs M6–M7 were coupled to something like a voltage equivalent to VDD, two times greater than the VDD/2 of its Strong ARM latch. The reduction in the quantity of stacked transistors is another benefit. Power supply voltage requirements are loosened as a result of this. In spite of the fact that the Miyahara's two-stage comparator boosts speed, this following method may make it faster even further. Since the electron mobility of pMOS transistors is much less than that of nMOS transistors (as shown in Figure 4.1), the regeneration speed of the latch input pair M6–7 is constrained. Consequently, Latch input pairs will be replaced with nMOS transistors in such an effort to considerably increase regeneration speed. Each input pair of preamplifiers' nMOS transistors must be preserved.

That three-stage comparison can be seen in this video. As an additional preamplifier stage, either latch stage but the very first preamplifier may be added as nMOS input pairs significantly speed up regeneration. There at beginning of both comparisons, because all these input pairs operate inside this saturation area, average input referenced noise was minimised. It's common to employ preamplifier gain that speed up transistor regenerative speed and decrease input-referenced offset & noise. As compared to the previous three-stage comparator, that performs better in terms of both speed and noise.

4. PROPOSED METHOD

That three-stage comparator shown in Fig. 2 is used in this study. One after another, these three steps link together. The basic difference between both the Miyahara's comparator and this one is the inclusion of a second preamplifier (the second stage) (the second stage). Rather than use a pMOS input pair, the additional preamplifier acts as an inverter, speeding up something both latch stage and the output stage.

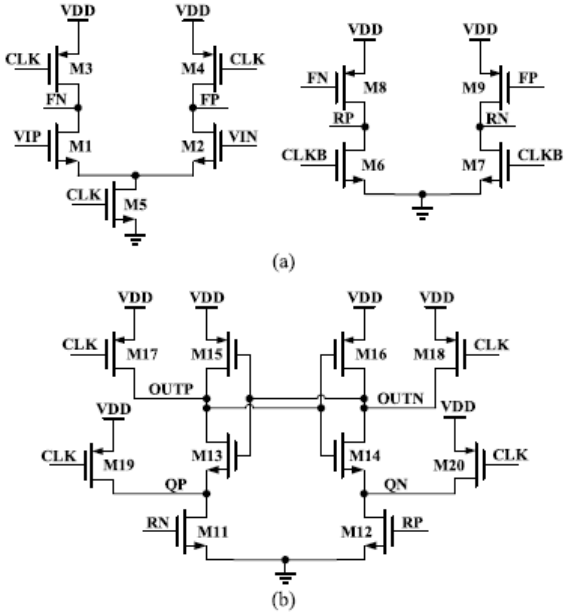

Fig.2. Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage).

To speed up its regeneration process and reduce the input-related offset & noise, an additional preamplifier offers voltage gain. In spite of this, the additional preamplifier aids in boosting the speed since these amplified signal now needs during two stages instead of only 1 previous to it reaches the latch stage. We need to weigh the advantages and disadvantages of this additional delay. In Fig. 5.1, this outputs FP and FN are connected to GND following the very first amplification. A substantial gate–source voltage, identical to VDD, is now present at the second-stage input pair M8–9. In order to fast raise RP & RN, the current on M8–9 is sufficient. As a result, the second stage's additional delay is little To put it another way, in compared to latch stage's considerable delay. since a second stage in such a active inverter doesn't add significant delay, which makes sense. Aside from that, the three-stage comparator's initial output load (Fig. 5.1) is only M8–9 compared to the M6–7 and M12–15 for Miyahara's comparator (Fig. 1). In order to increase the amplification rate, the output load was lowered by many orders of magnitude.

Miyahara's as well as the three-stage comparison are shown in Fig 5.2 in a transient simulation comparison. Clearly, the lower output load of both the three-stage comparator allows it to settle at 60 ps sooner than just the Miyahara's first-stage output in the first stage. According to 90% settling, this three-stage comparator's second-stage output is quicker than Miyahara's first-stage output through 40 ps, even taking into consideration the additional delay of both the second stage. These nMOS input pair also reduces the latch stage maintain current by 76 ps.

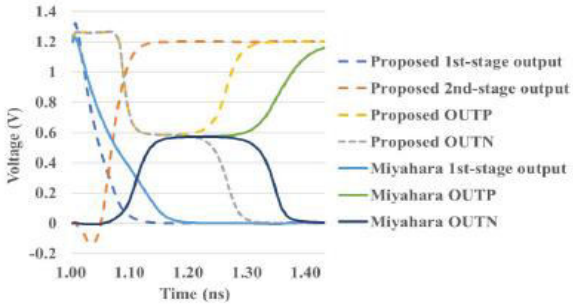

Fig. 3. Transient simulated waveforms of the Miyahara's comparator and the three-stage comparator

There are several advantages to using this three-stage comparison over the comparator in [12]. Figure 5.1 shows that the very first output of M6–7 is connected to CLKB, however this is incorrect, for two reasons: As a result, the output of the first stage has less parasitic capacitance. Second, instead of

being linked to the second-stage output, M17–20's gate is connected to CLK. Reduces its second-stage output capacitance by doing this. Clocked nMOS is removed from M1–2 in order to free up space on top of M1–2. The parasitic capacitance in the first stage is reduced by this method. At the same time, it ensures that the drain of M1–2 is set to VDD when comparing the two values. Input referred noise may be reduced by limiting the input pair's saturation zone. As a consequence of the input pair's assured saturation zone and lower parasitic capacitances, post-layout modelled results reveal a 15 percent reduction in input referenced noise and a 6 percent boost in speed.

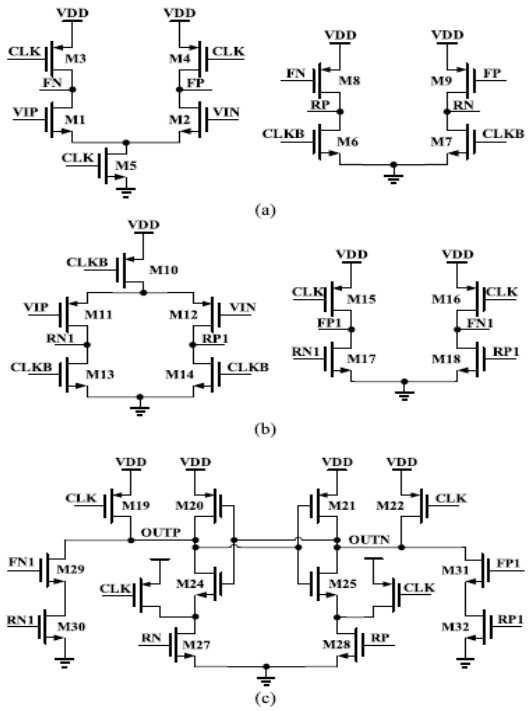

Fig. 4. Proposed modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

This brief suggests a customized form of the three-stage comparator, as illustrated in Fig. 5.3, with order to eliminate kickback noise & extra enhance the speed. The sole change between this updated version as well as the original is indeed the addition of Fig. 5.3(bfirst)'s two stages and Fig. 5.3's latch stage's additional routes M29–32 (c). This nMOS input pair M1–2 feedback noise was cancelled out by the pMOS input pair M11–12 throughout the extra first two stages.

Extra routes M29–32 provide additional signals to latching nodes OUTP as well as OUTN to even further boost regeneration speed as well as minimise input referred offset as well as noise.

These additional circuits work as follows. At the beginning of the reset, CLK and CLKB are both set to 1. It is seen in Figure 4(b) that GND is set for RP1 and RN1 & VDD is set for both FP1 & FN1. Fig. 4(c) shows how to switch off M30 and M32, which ensures that neither static current travels via the additional M29–32 circuit channel.

Amplification occurs when CLK increases to 1 while CLKB decreases to 0. Figure 4(b) shows that RP1 and RN1 increase to VDD (R stands for rise). FP1 and FN1 have finally brought to rest (F stands for fall). Response to the increases then falling of RP1 and RN1, there is a short-lived differential current draw out from latching nodes OUTP and OUTN. It is caused by the extra pathways in Fig.4(c).

OUTP & OUTN are connected at a differential voltage, thereby speeds up regeneration and reduces the comparator input reference offset as well as noise. Static current is prevented by turning off the additional routes in Fig. 5.3(c) when FP1 and FN1 have fallen to GND. A three-stage comparator with its output reference offset and noise reduced, as well as its kickback noise increased speed. These SAR ADCs might benefit from such a new technology.

According to this example, the modified version of the time-interleaved noise shaping SAR ADC was acceptable. An analog-to-digital converter's speed and resolution are both constrained by the comparator's

kickback noise. Complexity is indeed a drawback of using channel isolation to decrease kickback noise for Zhuang et al. [13]. The suggested three-stage comparator, on the other hand, may address these difficulties. When compared to other models, this one boasts the quickest response time and the quietest kickback noise.

5. RESULTS

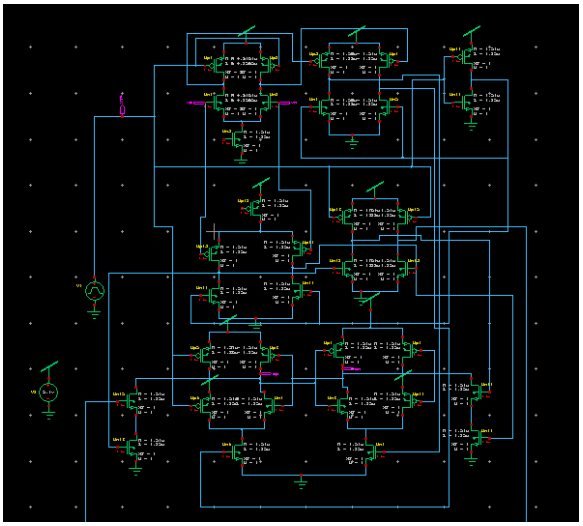

Fig 5 Circuit Diagram of Modified Three stage Comparator

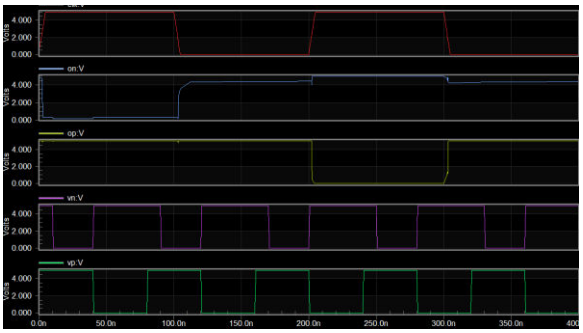

Fig 6 Simulation Wave from of Modified Three stage Comparator

6. COMPRESSION TABLE

	Two Stage Comparator	Three Stage Comparator	Modified version Three Stage Comparator
Delay	200.192ns	200.192ns	806.30ns
Speed	4.995Mhz	4.995Mhz	124Mhz
Power	3.739mW	3.031mW	3.022mW
Energy	748.532	606.78	24.36

7. CONCLUSION

This preamplifier gain may be adjusted using a specific clocking pattern in conjunction with a pMOS latch and pMOS preamplifier in the suggested comparator. Extremely low common mode voltage there at preamplifier outputs is maintained by using pMOS transistors somewhere at latch's input and a cross-coupled circuit. This results in a sufficient preamplifier gain. There is no kickback noise or input reference offset or noise inside the three-stage comparator as well as its modified version. Such comparators may well be useful for high-speed, high-resolution SAR ADCs. In the end, the results of the testing show that the comparators are effective.

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