

Approximate Multiplier Design Using Novel Dual Stage 4:2 Compressor

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ABSTRACT

High speed multimedia applications have paved way for a whole new area in high-speed error-tolerant circuits with approximate computing. These applications deliver high performance at the cost of reduction in accuracy. Furthermore, such implementations reduce the complexity of the system architecture, delay and power consumption. This model explores and proposes the design and analysis of two approximate compressors with reduced area, delay and power with comparable accuracy when compared with the existing architectures. The proposed approximate 4:2 compressor reduced in area, and reduction in delay. The proposed compressors are utilized to 16×16 Dadda multipliers. These multipliers have comparable accuracy when compared with state-of-the-art approximate multipliers.

1. INTRODUCTION

Numerous advanced applications require power proficiency. Also, these applications are implanted and additionally battery worked. Instances of such applications are Internet of Things (IoT) gadgets. These applications, for example, picture preparing, detecting, acknowledgment, and AI, are inalienably blunder lenient. Because of the way that exact outcomes are not generally needed, almost precise results typically get the job done. In this way, rough figuring [1] is one of the promising procedures for such applications to fulfill the need of low force utilization. Utilizing this method, force can be exchanged for exactness.

MULTIPLICATION

Multiplication is an essentially fundamental activity in applications, for example, the ones presented previously. In this way, lessening the expense of duplication benefits the previously mentioned class of utilizations. This venture centers around a rough multiplier. While a few inexact multipliers have been actualized [1, 2, 3, 4, 5], the scope of such applications is restricted in light of the fact that the greater part of the earlier works need exactness adaptability [2, 3]. Thus, dynamic configurability is essential, particularly for the accompanying two reasons.

Multipliers assume a significant part in the present computerized signal preparing and different applications. With progresses in innovation, numerous scientists have attempted and are attempting to plan multipliers which offer both of the accompanying plan targets – fast, low force utilization, consistency of format and henceforth less territory or even mix of them in one multiplier in this way making them reasonable for different high velocity, low force and reduced VLSI execution.

The regular augmentation technique is "add and move" calculation. In equal multipliers number of incomplete items to be added is the principle boundary that decides the exhibition of the multiplier. To diminish the quantity of fractional items to be added, Modified Booth calculation is perhaps the most famous calculations. To accomplish speed enhancements Wallace Tree calculation can be utilized to diminish the quantity of successive adding stages. Further by joining both Modified Booth calculation and Wallace Tree strategy we can see benefit of the two calculations in a single multiplier. Anyway with expanding parallelism, the measure of movements between the halfway items and moderate

entireties to be added will build which may bring about decreased speed, increment in silicon zone because of inconsistency of design and furthermore expanded force utilization because of expansion in interconnect coming about because of complex directing. Then again "sequential equal" multipliers bargain speed to accomplish better execution for territory and force utilization. The determination of an equal or chronic multiplier really relies upon the idea of use. In this talk we present the duplication calculations and design and analyze them as far as speed, territory, force and blend of these measurements.

2. LITERATURE SURVREY

A transistor level XOR-XNOR based low power design for 4 : 2 compressor was proposed by [1]. which is ideal for tree structured fast multipliers. Chang et al. have proposed a 4 : 2 and a novel 5 : 2 compressor that operates on low supply voltage of 0.6 V. [2] have proposed logic level approximation based architectures for 4 : 2 approximate compressor that are optimised for delay and power consumption. A re-configurable architecture for a 4 : 2 approximate compressor is proposed by [18], where the re-configurability is achieved by switching between approximate and accurate operations when required. [19] have proposed a 4: 2 approximate compressor that reduces the error profile of the compressor by introducing a module for error recovery. While performing the multiplication operation, truncation of n^2 columns (starting from right in the complete partial product array) is carried out. Compressors are applied only to the remaining columns. A probability driven approximate compressor is presented by Guo et al. The authors have proposed a top-down structure for an approximate multiplier which dynamically allocates between the 8 : 2, 6 : 2 and 4 : 2 approximate compressors based on the partial product count. As a measure to increase the accuracy of the multiplier, a grouped error recovery scheme is also proposed. [5] have presented an approximate adder based heterogeneous approximate multiplier with reduced MED. This is achieved by utilising the genetic algorithm based approximate adders. Esposito et al. have proposed an XOR-less (AND-OR based) compressor to minimise the average error and error probability. Chang et al. have proposed a 4 : 2 compressor to improve energy quality efficiency in image processing with 25% error rate. Gorantla and Deepa have proposed 4 : 2 and 5 : 2 compressors to reduce delay and power. Reddy et al. have proposed a novel design for 4 : 2 compressor with an error rate of 12.5%. This is achieved by relaxing the constraints on area, delay and power. Due to the considerable reduction in delay using transmission gates when compared to traditional CMOS based logic, optimised design with transmission gates are explored in literature. But, the major disadvantage is the inconsistency in the rise and fall times for different inputs. In this paper, two novel 4 : 2 compressor architectures are presented.

A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and Analysis of Approximate Compressors for Multiplication", Inexact (or approximate) computing is an appealing paradigm

For virtual processing at nanometric scales. Inexact computing is mainly thrilling for laptop mathematics designs. This paper offers with the analysis and design of two new approximate 4-2 compressors for utilization in a multiplier. These designs rely on distinctive functions of compression, such that imprecision in computation (as measured by means of the error charge and the so-known as normalized blunders distance) can meet with appreciate to circuit-based figures of merit of a layout (wide variety of transistors, postpone and power consumption). Four specific schemes for making use of the proposed approximate compressors are proposed and analyzed for a Dadda multiplier. Extensive simulation results are provided and an application of the approximate multipliers to photograph processing is offered. The results display that the proposed designs accomplish large discounts in electricity dissipation, put off and transistor count number in comparison to an precise layout; furthermore, two of the proposed multiplier designs provide exceptional talents for image multiplication with admire to common normalized mistakes distance⁴⁹ and top sign-tonoise ratio (more than 50 dB for

the taken into consideration photo examples).

C. Liu, J. Han, and F. Lombardi, "A Low-Power, High-Performance Approximate Multiplier with Configurable Partial Error Recovery", Proc. Of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), [Approximate circuits were considered for errors-tolerant packages which could tolerate some loss of accuracy with improved performance and power performance. Multipliers are key mathematics circuits in many such programs consisting of digital signal processing (DSP). In this paper, a novel approximate multiplier with a decrease electricity intake and a shorter essential direction than traditional multipliers is proposed for high-overall performance DSP packages. This multiplier leverages a newly-designed approximate adder that limits its carry propagation to the closest pals for immediate partial product accumulation. Different ranges of accuracy may be performed thru a configurable errors restoration by way of the use of distinctive numbers of maximum massive bits (MSBs) for errors discount. The approximate multiplier has a low suggest error distance, i.E., most of the errors are not vast in magnitude. Compared to the Wallace multiplier, a 16-bit approximate multiplier implemented in a 28nm CMOS manner suggests a reduction in postpone and power of 20% and up to 69%, respectively. It is proven that with the aid of utilising the suitable mistakes recuperation, the proposed approximate multiplier achieves similar processing accuracy as traditional genuine multipliers however with enormous improvements in electricity and performance.

3. PROPOSED METHOD

APPROXIMATE MULTIPLIER DESIGN USING NOVEL DUAL-STAGE 4: 2 COMPRESSORS:

Approximate multipliers are widely being advocated for energy-efficient computing in applications that exhibit an inherent tolerance to inaccuracy. However, the inclusion of accuracy as a key design parameter, besides the performance, area and power, makes the identification of the most suitable approximate multiplier quite challenging. In this paper, we identify three major decision making factors for the selection of an approximate multipliers circuit: (1) the type of approximate area efficient compressor and dual quality compressor used to construct the multiplier, the architecture, i.e., array or tree, of the multiplier and the placement of sub-modules of approximate and exact multipliers in the main multiplier module. Based on these factors, we explored the design space for circuit level implementations of approximate multipliers. We used circuit level implementations of some of the most widely used compressors.

EXACT 4:2 COMPRESSOR

The general block diagram of an exact 4 : 2 compressor is shown in Figure 1. It comprises of five inputs, three outputs and two cascaded full adders. A1, A2, A3, A4 and CIN are the inputs and COUT, CARRY and SUM are the outputs of the exact 4:2 compressor. COUT, CARRY and SUM are given as

$$COUT = A3(A1 \oplus A2) + A1(A1 \oplus A2) \quad (1)$$

$$CARRY = CIN (A1 \oplus A2 \oplus A3 \oplus A4) + A4(A1 \oplus A2 \oplus A3 \oplus A4) \quad (2)$$

$$SUM = CIN \oplus A1 \oplus A2 \oplus A3 \oplus A4 \quad (3)$$

A compressor chain is shown in Figure 1. CIN represents the input carry from the preceding 4 : 2 compressor that has processed the lower significant bits. CARRY and COUT are the outputs of order '1' with higher significance than the input CIN . Table 1 presents the truth table for the exact compressor.

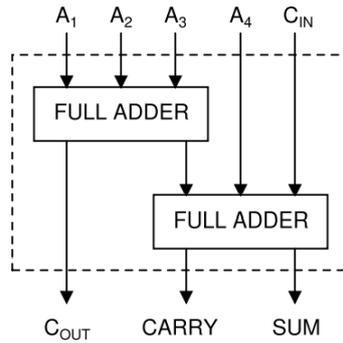


Fig.1: EXACT 4:2 COMPRESSOR.

Table 1. Truth Table For Exact 4:2 Compressor.

A ₁	A ₂	A ₃	A ₄	C _{IN}	C _{OUT}	CARRY	SUM
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	0	1	0	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	0	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

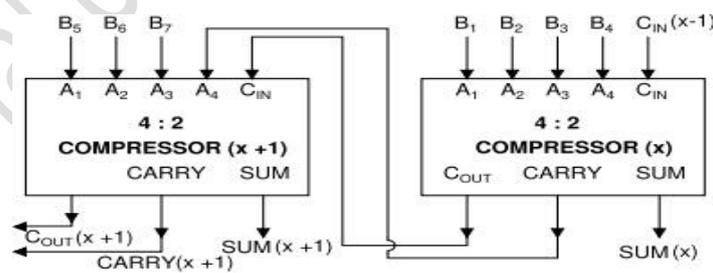


Fig. 2: Compressor chain.

AREA-EFFICIENT APPROXIMATE 4:2 COMPRESSOR

The proposed high speed area-efficient 4:2 approximate compressor is shown in Figure 3. The compressor inputs are A₁, A₂, A₃ and A₄, outputs are CARRY and SUM. A multiplexer (MUX) based design approach is used to generate SUM. Output of XOR gate acts as the select line for the MUX. When select line goes high, (A₃A₄) is selected and when it goes low, (A₃ + A₄) is selected. By introducing an error with error distance 1 in the truth table of the exact compressor, the proposed 4 : 2 compressor is able to reduce carry generation logic to an OR gate. The logical expressions for realisation of SUM and CARRY are given below.

$$\text{SUM} = (A_1 \oplus A_2) A_3 A_4 + (A_1 \oplus A_2) (A_3 + A_4) \tag{4}$$

$$\text{CARRY} = A_1 + A_2 \tag{5}$$

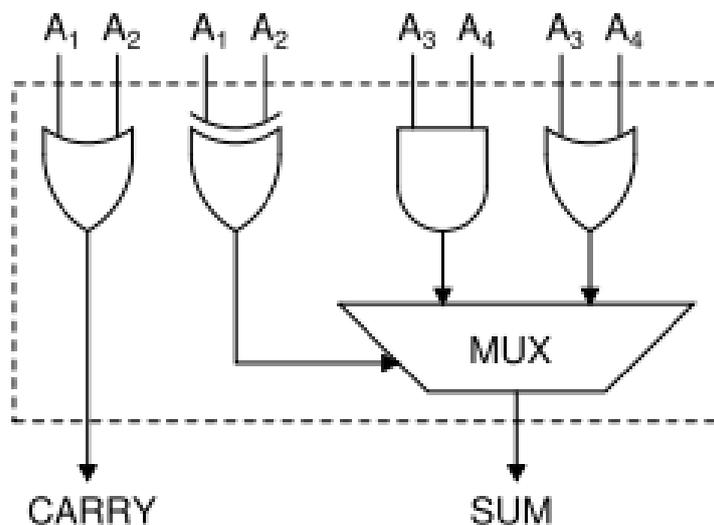


Fig. 3: Area-efficient 4:2 compressor.

From the truth table of proposed 4:2 compressor (Table 2), it can be observed that the error has been introduced for the input values – {0011}, {0100}, {1000} and {1111}, so as to ensure that equal positive and negative deviation with ED = 1 (minimum) is obtained.

TABLE 2. Truth table for proposed area efficient 4:2 compressor.

A ₁	A ₂	A ₃	A ₄	CARRY	SUM
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

DUAL-STAGE APPROXIMATE 4 : 2 COMPRESSOR

As a measure to optimise the hardware utilisation of the proposed design, this paper proposes an alternate architecture for multipliers with more than three stages of cascaded compressors. In the high speed area-efficient compressor architecture (as shown in Figure 3), apart from the MUX, one XOR, one AND and two OR gates are required. OR and AND gates each need 6 transistors in CMOS logic implementation. In order to reduce the transistor count, this paper proposes an architecture with NAND and NOR gates as shown in Figure 4. Even though the SUM and CARRY generated by the modified architecture is not as same as that of the proposed 4 : 2 compressor architecture, with cascading of the compressor in multiples of 2, the error is nullified. This is explained with the help of Figure 5. Figure 5(a) has a two level cascading of proposed high speed area-efficient 4 : 2 compressors.

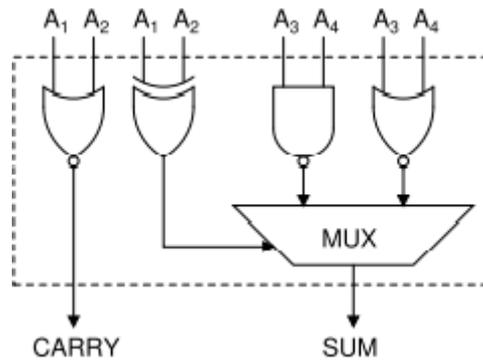


Fig. 4 Basic building block for proposed modified Dual-stage 4:2 compressor.

Figure 4 has a two level cascading of modified dual-stage 4 : 2 compressors. The outputs at the Stage 1 differ for both the architectures, but the occurrence of negation in the order of an integral multiple of two (in Stage 1 and Stage 2) in the modified dual-stage 4 : 2 compressor will ensure that the outputs at Stage 2 are same. The modified dual-stage 4 : 2 compressor reduces area, delay and power dissipation compared to the proposed high speed area-efficient 4 : 2 compressor and other compressors in the literature due to the reduction in transistor count. Table 3 analyses the output of the two proposed architectures at different stages in a 2 stage cascaded structure. Carry0 at Stage 2 output is minimised and is given in equation. $(K3 \oplus K4) \cdot (K2 + K1) + (K3 \oplus K4)(K2K1) = (K3 \oplus K4) \cdot (K2 + K1) + (K3 \oplus K4) \cdot (K2K1) + (K2 + K1)(K2K1)$ Here, it is seen that $(K2 + K1)(K2K1)$ is not an essential prime implicant. Therefore, output expressions of Stage 2 for both the proposed architectures are the same. Similarly, Sum0 generated

G. Zervakis, et al., “Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation” Approximate computing has acquired significant interest as a promising approach to decrease strength consumption of inherently error tolerant applications. In this paper, we cognizance on hardware-level approximation by introducing the partial product perforation technique for designing approximate multiplication circuits. We prove in a mathematically rigorous manner that during partial product perforation, the imposed mistakes are bounded and predictable, depending only on the input distribution. Through massive experimental evaluation, we observe the partial product perforation approach on special multiplier architectures and disclose the most excellent structure-perforation configuration pairs for distinct mistakes constraints. We show that, as compared with the respective actual design, the partial product perforation grants discounts of as much as 50% in power consumption, 45% in location, and 35% in vital put off. In addition, the product perforation method is as compared with the contemporary approximation techniques, i.E., truncation, voltage overscaling, and logic approximation, displaying that it outperforms them in phrases of strength dissipation and error.

T. Yang, T. Ukezono, and T. Sato “A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design”, Multiplication is a key essential function for plenty errors- tolerant programs. Approximate multiplication is taken into consideration to be an green approach for buying and selling off electricity against performance and accuracy. This paper proposes an accuracy-controllable multiplier whose very last product is generated through a convey-maskable adder. The proposed scheme can dynamically pick the period of the convey propagation to meet the accuracy necessities flexibly. The partial product tree of the multiplier is approximated with the aid of the proposed tree compressor. An eight \times 8 multiplier design is implemented by using the convey maskable adder and the compressor. Compared with a traditional Wallace tree multiplier, the proposed multiplier reduced energy consumption by between forty seven.3% and 56.2% and important route delay by way of among 29.9% and 60.5%, relying on the specified accuracy. Its silicon place turned into additionally forty four.6% smaller. In addition, outcomes from an picture processing software demonstrate that the great of the

processed photos may be controlled by using the proposed multiplier layout.

4. RESULTS

RTL SCHEMATIC: The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development. The hdl language is used to convert the description or summary of the architecture to the working summary by use of the coding language i.e., verilog, vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing. The figure represented below shows the RTL schematic diagram of the designed architecture.

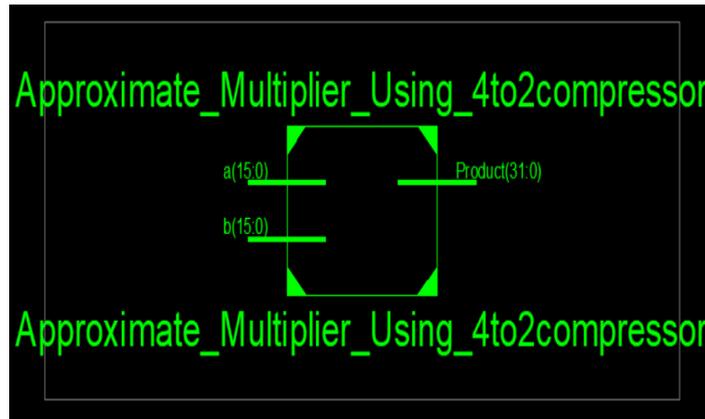


Fig. 5: RTL SCHEMATIC OF THE PROPOSED DESIGN

TECHNOLOGY SCHEMATIC:- The technology schmatic makes the reesentation of the architecture in the LUT format ,where the LUT is consider as the parameter o area that is used in VLSI to estimate the architecture design .the LUT is consider as an squarunit the memory allocation of the code is represented in there LUT s in FPGA

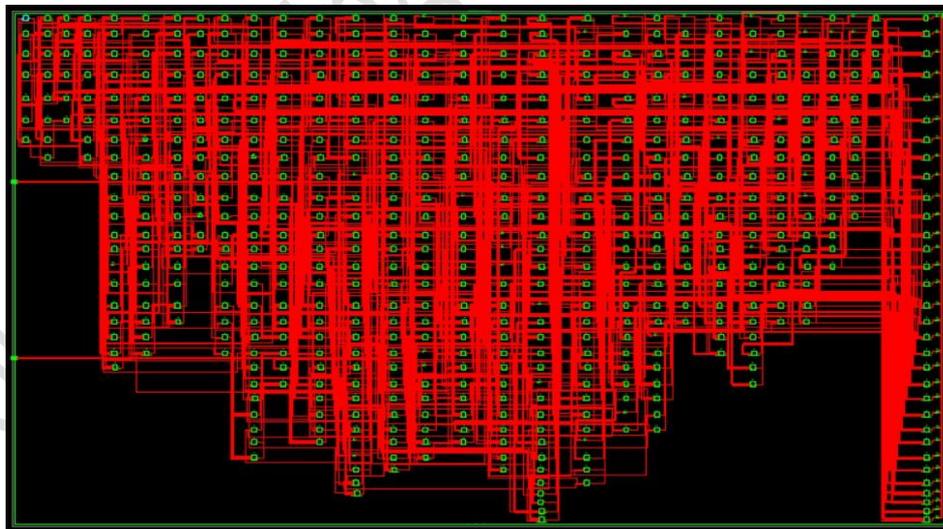


Fig 6 Technology Schematic Of The Proposed Design

SIMULATION: The simulation is the process which is termed as the final verification in respect to its working where as the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implantation to the simulation on the home screen of the tool ,and the simulation window confines the output in the form of the wave forms. Here it has the flexibility of providing the different radix number systems.



Fig 8: Simulation wave forms of proposed approximate multiplier

Table 3: power analyzer

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device	Spartan3e	On-Chip	Power (W)	Used	Available	Utilization (%)	Supply	Summary	Total	Dynamic	Quiescent		
Family	xc3s100e	Logic	0.000	133	1920	7	Source	Voltage	Current (A)	Current (A)	Current (A)		
Part	vq100	Signals	0.000	146	--	--	Vccint	1.200	0.008	0.000	0.008		
Package	Commercial	IOs	0.000	33	66	50	Vccaux	2.500	0.008	0.000	0.008		
Temp Grade	Typical	Leakage	0.034				Vcco25	2.500	0.002	0.000	0.002		
Process	-5	Total	0.034										
Speed Grade													
Environment		Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)		Supply Power (W)	Total	Dynamic	Quiescent			
Ambient Temp (C)	25.0		49.0	83.4	26.6			0.034	0.000	0.034			
Use custom TJA?	No												
Custom TJA (C/W)	NA												
Airflow (LFM)	0												
Characterization													
PRODUCTION	v1.2.06-23-09												

Consider in VLSI the parameters treated are area, delay and power, based on these parameters one can judge the one architecture to other. here the consideration of area power and delay also considered the parameter is obtained by using the tool XILINX 14.7 and the HDL language is verilog language.

5. CONCLUSION

This project presents approximate multiplier with novel approach of approximate 4: 2 compressor architectures. Firstly, a high speed area efficient compressor architecture is proposed, which achieved a considerable reduction in area, delay and power when compared to other state-of-the- art compressor designs. The proposed design has comparable accuracy .As a result, the proposed design reduces area power and delay also. In addition to this, the model also proposed a modified dual-stage compressor architecture, which further optimized the area, delay and power without altering the accuracy metrics. The architecture was designed and 16 × 16 Dadda multiplier in image processing applications, like image multiplication and smoothing.

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