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DESIGN OF LOW POWER FSM BASED VENDING MACHINE USING XILINX

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***Abstract*—** In this paper the central idea of this work is to design a vending machine that will be able to provide a number of items like soft drink, cake &cold rinks to people. The machine will also deliver the change, depending on the amount of money inserted and the price of product. At the same time we have made efforts to make the design of the Vending Machine power efficient by using power reduction techniques. In this process we have tested our design at different frequencies and analyzed the consumed power. Next, we have also calculated the power at different frequencies with different IO STANDARD like LVCMOS33, LVCMOS12, SSTL18BI, HSTLBIB18. The proposed design is tested and implemented using VERILOG HDL and XILINX ISE 14.2targeting XC3S500E FPGA. The result shows optimization of power.

Keywords: Verilog, lvcmos33, iostandard,sstl18bi, hstlbib18.

I. INTRODUCTION

Vending Machine is a product used to dispense various products like candy, cold drinks, cakes etc. when desired amount of money is inserted into it. The Vending Machine is more accessible and practical then conventional purchasing method. Nowadays, Vending Machine can be seen everywhere near ATMΓs, Metro Stations, Movie Theatres and many more places. These are handier as they are accessible 24k7[7]. it also helps in reduction of overhead costs by not hiring of staff increases profit margin. They can also be moved to other places in case the situation arises and they will continue performing in the same manner as it was performing earlier. In most of the papers based on vending machine, the main focus is to increase the number of products, as well as the speed of computation of the machine. But increase in computational speed as well as by increase in quantity of products is possible only through increased hardware which leads to high power consumption that keeps on increasing due to development in VLSI technology. In this paper we have discussed some techniques for reduce power at the architectural level to make my design of Vending Machine more efficient in terms of power.

FPGA is a Silicon chip containing two dimensional arrays of logic blocks and with electrically programmable interconnects [8]. The main reason behind choosing our platform as FPGA instead of any microprocessor is the advantage it posses i.e. of it can be reprogrammed at any time .with different functionality each time [9]. Moreover if any one made an error in his design he can just fix that logic, recompile it and redownload it on your FPGA Board, no need for soldering or no need to change the components. The speed of computation is also very fast in FPGA. The Vending machine is based on the concept of FSM. There are only two types of state machines, and moor model. the output depends on the input as well as the present state. The output depends only on the present state.

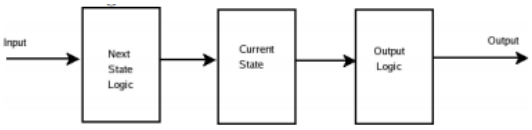

Figure-1: More Machines

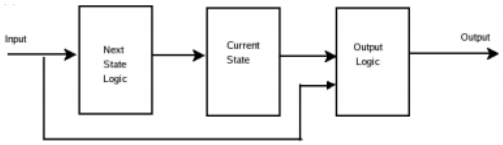

Figure-2: Mealy Machines

II. RELATED WORK

a) mishra s, verma G. Ilow power and area efficient implementation ofBcD adder on FpGa", international conference on signal processingand communication (icscY2013); 2013 Dec 12Y14; Jiit, noida: ieeeΓXplore; 2013. p. 461-5

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Decimal adders and multipliers are the basic building block for arithmetic and logical unit and barrel shifters in today's high end processors and controllers. In this paper, an efficient BCD adder is designed based on low power synthesis technique at the architectural level. There are different levels of abstraction at which the power can be minimized but the low power technique at the architectural level has more impact than that of circuit level approaches. Two different approaches have been discussed i.e. pipelining and parallelism, so as to minimize the power consumption at architectural level. The proposed designs are tested and implemented using VHDL and the Xilinx ISE 10.1 targeting Xilinx XC5VLX30-3 FPGA. The result shows the optimization of power, delays and the area for different designs and a comparison analysis is provided based on the existing designs in the literature.

b) Gauravverma, shambhavimishra, sakshiaggarwal,surabhisingh, sushants hekhar and sukhbanikaurvirdi, I power consumption analysis of BcD adder using X power analyzer on vertex Fpga", Indian Journal of science and technology, vol 8(18), ipl0160, august2015

Adders are the integral part of any digital circuit operation. Optimization of adder's supremacy along with its vicinity is a demanding chore. In this work an efficient BCD ADDER1 is analyzed in terms of power consumption by scaling the various parameters like voltage, frequency and load capacitance. In addition to this the focus is also given on the airflow of the device to reduce the power. Finally the power is reduced by sending different encoded data at the input. The proposed designs are hardened and implement by means of VHDL and Xilinx ISE (integrated Software Environment) 14.5 and validated using XPower targeting Virtex FPGA. Power consumption is discussed in terms of clock, signals, logic, input/ outputs and leakage. A comparative analysis has been shown at the end to validate the obtained results.

III. IMPLEMENTATION OF VENDING MACHINE

In this paper a state diagram is constructed for the proposed machine which can vend four products that is coffee, cold drink, candies and snacks. Four select (select1, select2, select3) inputs are taken for selection of products. Select1 is used for the selection of snacks. Similarly select2, select3, are used for coffee, cold drink and candies respectively. Rs_05 and rs_10 inputs represents rupees 15/- notes respectively. A cancel input is also used when the user wants to withdraw his request and also the money will be returned through the return output. Return, product and change are the outputs. Return and change vectors are seven bits wide. Money is an in/out signal which can be updated with the total money of all products delivered at a time. Money signal is seven bits wide. Money_count is an internal signal which can be updated at every transition. This signal is also seven bits wide. If the inserted money is more than the total money of products then the change will be returned through the change output signal. The products with their prices are shown by table 1. There are also two input signal clk and reset. The machine will work on the positive edge of clock and will return to its initial state when reset button is pressed. The proposed vending machine is designed using FSM modelling and is coded in VHDL language.

IV. DESIGN METHODOLOGY

i) the user first selects the item he wants to purchase.
ii) then the user inserts the money.
iii) if the money inserted in the machine matches to that of theproduct selected then the product is dispensed as the output.
iv) if there is any change left it is given back to the user. in myvending machine there are only 3 types of product withtheir prices given below in table 1:

Table 1: product with their prices

S.NO	PRODUCT	PRICE
1	CANDY	5
2	CAKE	10
3	COLDRINK	15

From the figure 3 it is clear that vending machine only accepts two types of coins i.e. coinB5 (for a 5 rupee coin) and coin B10(for a 10 rupee coin). Four types of select bit are also present for the user i.e.
i) SB0: initially it will be present in idle state or reset state.
ii) SB1 (2Γb01): for the selection of product candy.
iii) SB2 (2Γb10): for the selection of the product cake.

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iv) SB3 (2Γb10): for the selection of the product cold drink.

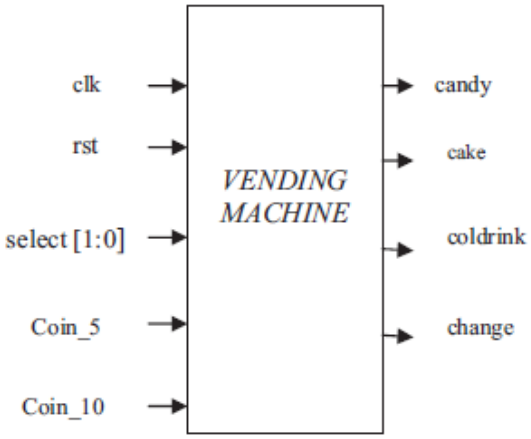

Figure-3: Block diagram of Vending Machine

Vending machine has also five intermediate states.
i) StB0(if it is in state zero)
ii) StB5(if it is in state five)
iii) StB10(if it is in state ten)
iv) StB15(if it is in state fifteen)
v) StB20(if it is in state twenty)
the FSM of cold drink, candy, cake are shown in figure 4, 5 and 6 respectively.

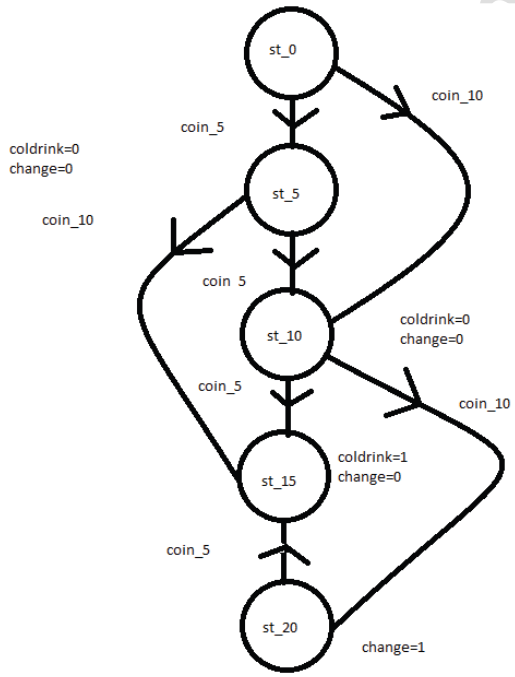

Figure-4: FSM for cold drink

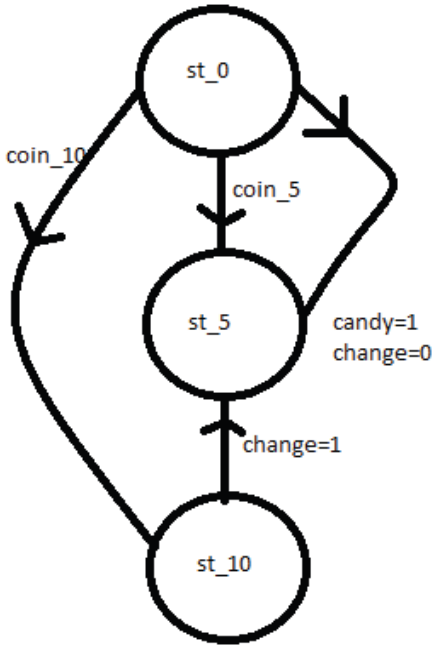

Figure-5: FSM for candy

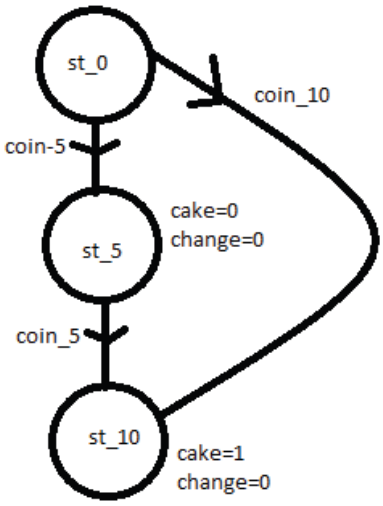

Figure-6: FSM for cake

V. RESULTS

RTL Schematic: RTL schematic is described as register transfer logic that means the logic is transferred to registers it is also known as designer view because of it is looking like what is the intension of designer.

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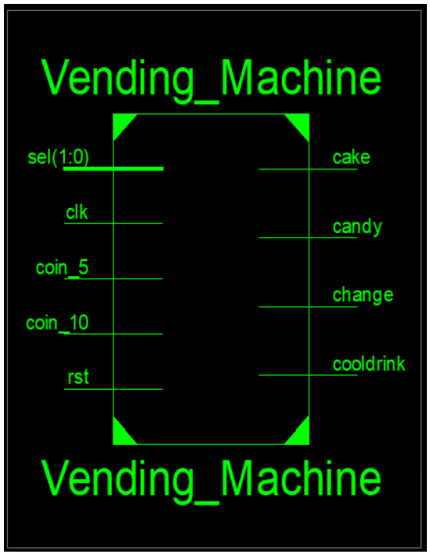

Figure-7: RTL Schematic of Vending Machine

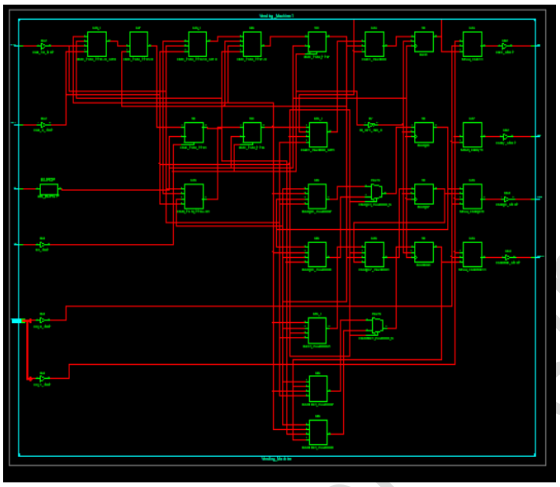

Figure-8: View Technology Schematic of Vending Machine

Figure-9: Simulated wave form of vending machine for candy when 5 rupee coin insert

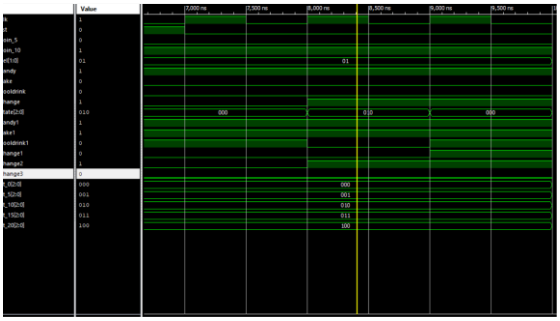

Figure-10: Simulated wave form of vending machine for candy when 10 rupee coin insert

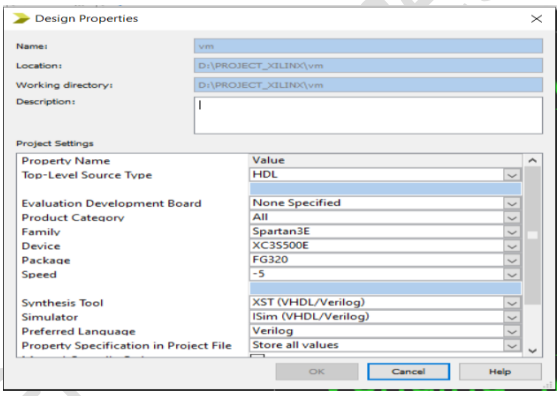

Figure-11: Device preferred for simulation

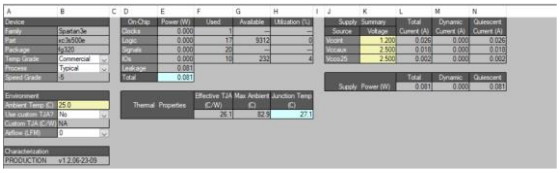

Figure-12: Power consumption for spatan3e

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	7	9,312	1%
Number of 4 input LUTs	17	9,312	1%
Number of occupied Slices	9	4,656	1%
Number of Slices containing only related logic	9	9	100%
Number of Slices containing unrelated logic	0	9	0%
Total Number of 4 input LUTs	17	9,312	1%
Number of bonded IOBs	10	232	4%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	3.65		

Figure-13: Hardware utilization summery

Minimum period: 2.928ns (Maximum Frequency: 341.565MHz)
Minimum input arrival time before clock: 3.562ns
Maximum output required time after clock: 5.255ns
Maximum combinational path delay: 5.895ns
Power consumption 0.1478m.watt.

VI. CONCLUSION

The vending machines that are popularly used till date are operated by receiving specific denomination i.e. The cost of the product and deliver it. They don't work when combinations of coins are inserted or more or less amount is given. But this vending machine is a solution for the above problems. It will deliver the product even if we insert more than the cost of the product and give the remaining change. It also delivers the product if we insert the amount in combination of coins. Some further developments are to be made to accept the currency notes also.

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