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Design of higher order Multiplier 32-bit with Approximate Compressor

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Abstract: ***Consumers demand for increasingly portable, high performance multimedia and communication products. This forces strict constraints on the power consumption of individual internal components. Most of the internal components of DSP are multipliers. Embedded application become essential to design more power aware multipliers. The basic building block of the multipliers can be used either in two ways. First it can be used as independent smaller precision multipliers else it can be used as work in parallel to perform high precision multipliers. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. Optimizing the speed and area of the multiplier is a major design issue. However, area and speedare usually conflicting constraints so that improving speed results mostly in larger areas. Various types of multiplications such as fixed length multiplication and multiprecision multipliers with 3 sub-block and 4 sub-block multipliers is to enhance power and area. Booth radix4 Wallace tree adder algorithm is used in the 32X32 bit fixed width multiplier and multiprecision multipliers with 4 sub-blocks and 3 sub-blocks. Silicon area is optimized by applying operation reduction techniques that replaces a multiplier by adders/subtractors. Synthesis can be done by means of Xilinx ISE design suite 8.1 and Modelsim can be used for simulation.***

Keywords: FWM, MPM, Xilinx ISE design suite 8.1 and Modelsim 6.3.

1. Introduction

Multipliers form an important hardware block in the DSP and Embedded applications. Multiplication speed determines processor speed. So high speed multipliers are needed in the processors for many applications. For increase the speed of multiplication different algorithms are used Multiplication is a most commonly used operation in many computing systems. A number (multiplicand) is added to itself a number of times as specified by another number (multiplier) to form a result (product). But the implementation of multiplier takes huge hardware resources and the circuit operates at low speed. Multiplication is oneof the fundamental components in DSP and Embedded system. A system‟s performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the real time system. Multiplier requires more hardware resources than the adder and substractors. For Improving the performance and reducing the power dissipation of the systems are the most important design challenges for Embedded and DSP applications. Increasing the word length results in hardware complexity and also increases the multiplication time. Many algorithm have been developed in order to realize high speed multipliers such as Booths algorithm, Wallace tree algorithm etc. Multipliers based on Booth algorithm and Wallace tree addition is one of the fast and low power multiplier. Multiplication consists of three major steps: 1) re-coding and generating partial products 2) reducing the partial products by partial product reduction schemes to two rows and 3) adding the remaining two rows of partial products by using a carry-propagate adder (e.g. Carry look ahead adder) to obtain the final product.

Booth‟s algorithm is used for multiplying unsigned numbers. It is a multiplication algorithm that utilizes two‟s complement notation of signed binary numbers for multiplication. An 8 bit multiplication computed on a 32 bit booth multiplier would result in unnecessary switching activity and power loss. With the reuse of 8 bit multiplier in 16 bit multiplication we can reduce the area overhead. The Wallace tree method is used in high speed designs in order to produce two rows of partial products that can be added to last stage. Also critical path and the number of adders get reduced when compared to the conventional parallel adders.

2. Overview of Multiplier

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has an important part in low-power VLSI system design. A system is generally determined bythe performance of the multiplier because the multiplier is generally the slowest element and more area consuming in the system. Hence optimizing the speed and area of themultiplier is one of the major design issues. However, area and speed are usually conflicting constraints so that improvements in speed results in larger areas. Multiplicationis a mathematical operation that include process of addingan integer to itself a specified number of times. A number (multiplicand) is added itself a number of times as specified by another number (multiplier) to form a result(product). Multipliers play an important role in today‟s digital signal processing and various other applications. Multiplier design should offer high speed, low power consumption. Multiplication involves mainly 3 steps

1) Partial product generation
2) Partial product reduction
3) Final addition

If the multiplicand is N-bits and the Multiplier is M-bits then there is N* M partial product. The way that the partial products are generated or summed up is the difference

between the different architectures of various multipliers. Multiplication of binary numbers can be decomposed into additions. Consider two unsigned binary numbers „X" and „Y" that are „M" and „N" bits wide, respectively. To introduce the multiplication operation, it is useful to express X and Y in the binary representation. Equation for the multiplication is

$$X(k) = \Sigma_{i=0}^{M-1}\Sigma_{j=0}^{N-1} a_i b_j 2^{i+j}$$

Multiplication Algorithm

1) If the LSB of Multiplier is 1, then add the multiplicand into an accumulator.
2) Shift the multiplier one bit to the right and multiplicand one bit to the left.
3) Stop when all bits of the multiplier are zero.

For designing a multiplier circuit we should have circuitry to provide or do the following three things:

1) It should be capable of identifying whether a bit 0 or 1 is.
2) It should be capable of shifting left partial products.

3. System Design

A) Fixed Width Multiplier

In the fixed width multiplier, the length of the multiplier and multiplicand bits are same. Block diagram of multiplier is shown in figure 1. The block diagram consists of Booth encoder, partial product generator, Wallace tree adder. Wallace tree adder consists of 3-2 compressor module and carry look ahead adder. Here "x" and "y" are the multiplier and multiplicand respectively. The booth encoder encodes the multiplier bits "x" and derive the encoded signal. The partial product generated according to the encoded signal. The partial product obtained from the multiplicand bits "y" as per the Booth Radix 4 algorithm. The summation of the partial product is according to Wallace tree algorithm. In WT algorithm, partial products are grouped in to stages. Each stage consists of three rows of Partial products and is applied to the carry save adder. In the final stages consist of two Rows of partial product and are applied to carry look ahead adder. The output from the carry lookahead adder is the multiplication result.

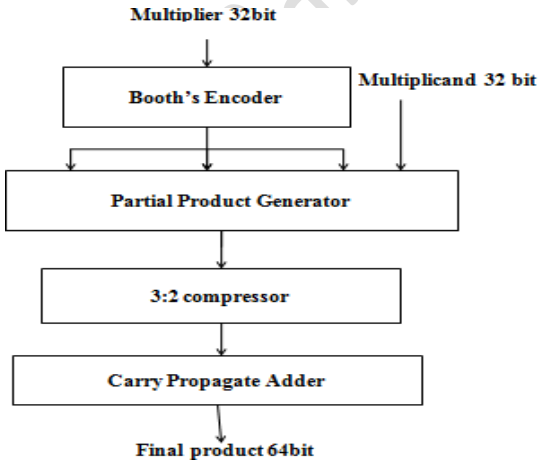

Figure 1: 32 bit fixed width multiplier

B) Multiprecision Multipliers

In the Multiprecision multipliers, multiplier comprises 8X8 multipliers work in parallel to perform 16X16 and 32X32 bit multiplication according to user"s constraints. Whenever the full precision (32 bit) is not needed the some of the 8X8 multipliers become inactive. 8X8 multipliers can be active/inactive according to the actual work load given.

Multiprecision multipliers with 4 sub-blocks

Let „X" and „Y" are the multiplier and multiplicand respectively. X_H and Y_H are the most significant bits wit „n" bit wide. X_L and Y_L are "n" least significant bits. The 4 sub-block consists of four n x n multipliers .The multiplication is done by Booth radix 4 WT algorithm. Multiplier structure is shown in the figure 2

$P = (X_HY_H)2^{2n} + (X_HY_L + X_LY_H)2^n + X_LY_L$ (1)

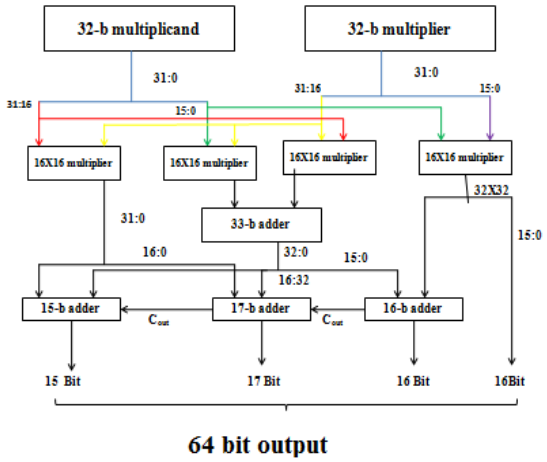

Figure 2: 32X32 bit multiplier

C) Multiprecision multipliers with 3 sub-blocks

Multiplier consist of two 16X16 multiplier and one 17X17 multiplier. The 32X32 bit multiprecision with 3 sub-block replaces a 16X16 bit multiplier with 34 bit subtractors. Multiplier Structure as shown in the figure 3

$X' = X_H + X_L$ (2)
$Y' = Y_H + Y_L$ (3)
$P = (X_HY_H)2^{2n} + (X'Y' - X_HY_H - X_LY_L)2^n + X_LY_L$ (4)

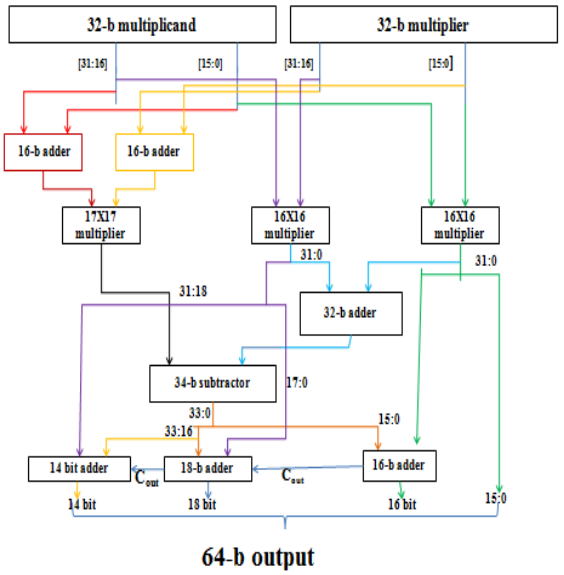

Figure 3: 32X32 bit multiplier

4. Results and Discussion

A. Simulated Result

Fixed width Multiplier

In the fixed width multiplier „x" and „y" are the input and „z" is the output.

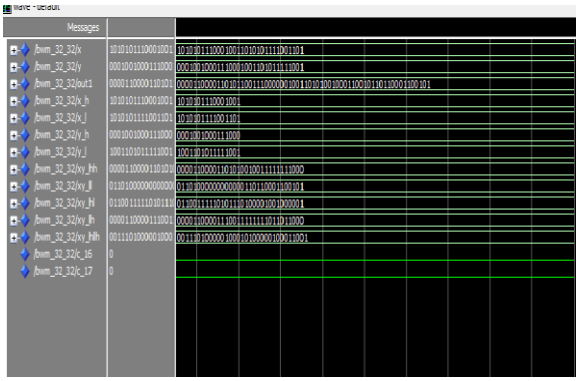

Figure 4: simulation of fixed width multiplier

Multiprecision multipliers with 4sub-block

In the multiprecision multipliers „x" and „y" are the input and „out1" is the output.

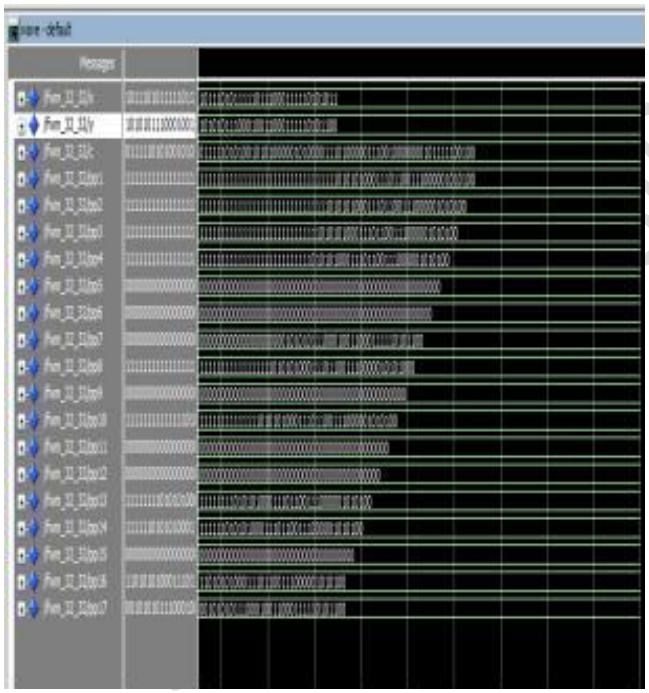

Figure 5: simulation of Multiprecision multiplier(4 sub-block)

Multiprecision multipliers with 3 sub-block

In the multiprecision multipliers „x" and „y" are the input and „z" is the output.

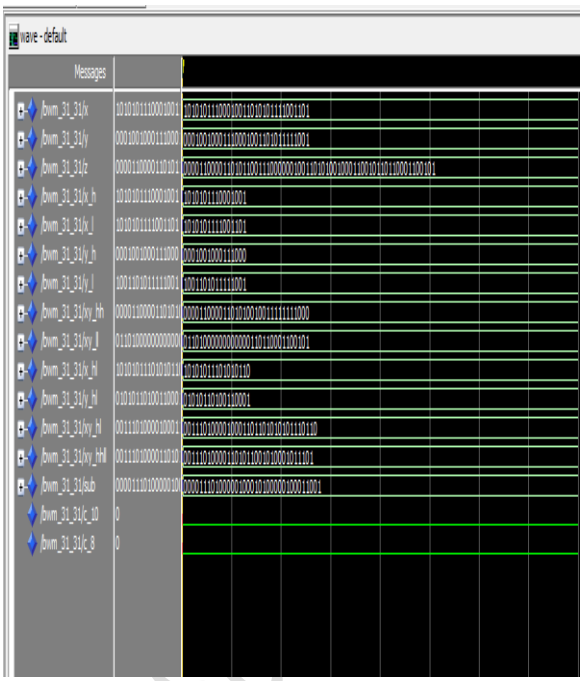

Figure 6: Simulation of multiprecision multiplier with 3 sub-block

Synthesis Report of Multipliers

Table 1: Synthesis report of multipliers

Components	FWM	MPM (4 Sub-block)	MPM(3 Sub-block)
Power(mw)	80	81	68
Area(LUT count)	2381	2936	2301

Table 1 shows the synthesis report of three multipliers.The multiprecision multiplier with 3 sub-block can achieve reduction of area and power compared with the FWM and MPM with 4 sub-block

5. Conclusion

Multipliers are the most important hardware block of a computing device . Hence the speed of a multiplier is a factor affecting the performance of a device. For a system to be designed appropriately the speed of the multiplier should be high and the area should be less. By considering all these factors, three types of multipliers were designed. The fixed length multiplier is designed to handle the multiplication of fixed length. Area utilization became inefficient when 32 bit fixed length multiplication is used for 8 bit multiplication. Hence the use of multiprecision multiplier 4 sub-blocks solve this problem by utilizing the area completely, but power cannot be reduced. In the multiprecision multiplier which was designed secondly, the area and power is reduced and the performance is increased. The most efficient multiplier designed is the 3 block multiprecision multiplierin which the power can be reduced by scaling the voltageand frequency. Similarly, the use of 4-2 compressor canreduce the area. In this manner, a good multiplier can be designed by reducing the area and power and by improving the performance.

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