JES Journal of Engineering Sciences

Vol 13, Issue 06, June/2022

ISSN NO:0377-9254

Design of High Speed 32-Bit Multiplier Using 10:2 Compressors And Its Application In Image Processing

[1]Mudunuri Bindu Madhuri, [2]Biswaranjan Barik,

[1,2] Department of ECE Godavari Institute of Engineering and Technology, Rajahmundry, Andhra Pradesh

[1]binduvarma11@gmail.com, [2] ranjan@giet.ac.in

ABSTRACT

At present, approximate multiplies are used in the image processing applications. These approximate multipliers are designed with the help of higher order compressors to reduce the number of addition stages involved in the reduction stages. In this paper, 10:2 compressors are designed and implemented in the 32-bit multiplier and compared with the exact 32-bit multipliers. The proposed multiplier is used for implementing FIR filter resulted 27ns delay which is far better than the exact multiplier having 119ns. These multipliers also used in image processing applications and PSNR of image has been employed. Using approximate multiplier we got PSNR value of resulted image as 21.14 db where as in exact multiplier PSNR value is 18.41 db.

Keywords: Compressor, Approximate multiplier, FIR filter, PSNR.

1. INTRODUCTION

In digital signal processing applications multipliers plays a vital role in the complex arithmetic operations. Here, the approximate computing techniques are used to reduce the power consumption. Hence approximate multipliers came into the existence and these approximate multipliers are widely used in the Digital Signal Processing applications to reduce the power consumption. The complex multipliers used in the DSP applications are replaced with these approximate multipliers. These can perform multiple operations like filtering, convolution, and correlation of the digital signals. To perform these complex multiplications multipliers, adders and shifters are widely used. Here, designing of the multiplier is the hardest part in the design of the DSP. These multipliers consume more power compared with the remaining adders and shifters.

In multiplication process there is a generation of partial products, alignment of partial products, and lessens the partial products and finally addition of all these partial products. Reducing the partial products count requires more time and power consuming. Multiple techniques are implemented to overcome this issue. The approximate computing technique gives the better results compared to all the previous techniques. Hence approximate adders came into existence and then compressors are designed for the addition of multiple bits. Higher order compressors are required to reduce the partial products and reduce the delay of the addition process. With the use of these approximate compressors approximate multipliers are designed to improve the performance of the Digital Signal Processing applications.

The exact multipliers are consuming high speed and require huge delay to obtain exact outputs. Due to these exact multipliers there is only one major defect is that it can't optimize further while using multiple techniques. Hence for the image processing and signal processing applications accept the errors data and gives the modulated signals. Hence approximate compressors and multipliers came into existence and reduce the power consumption and delay due to the reduction of the carry bits in the addition process. Due to these approximate multipliers approximate results are obtained and these are sufficient for the combining of the two signals.

The approximate compressors are designed to reduce the computation occurred in the addition process. Hence more number of inputs are added to produce only two outputs called as sum and carry bits and another one more output is also attained called as carry out. In general 4-2 compressors are widely used and these give the better results when compared to the previous architectures. Hence with the use of these approximate compressors the partial products are gets reduced and the adder count (gate count) is also reduced. The approximate multipliers need some extra compressors to improve its performance. Then the higher order compressors came into the existence and 10-2 compressors are designed. In this paper, a new 32x32 bit approximate multiplier is designed with higher order compressor achieves low power consumption and lesser delay along with the less error rate.

In this paper, the proposed design shows better performance instead of previous multipliers. The rest of the paper is organized as follows. The higher order compressors are implemented in section (II). The architecture of

32x32 bit multiplier using proposed 10:2 compressor is explained in section (III). Implementation Results are shown in section (IV). FIR implementation and image multiplication applications are implemented with proposed multiplier is shown in section (V). Finally conclusion is presented in section (VI)

2. DESIGN OF COMPRESSORS

A compressor is a combination circuit having multiple inputs and multiple outputs, the outputs consists of one sum bit and one carry bit along with these multiple carry propagating bits are also generated according to their input bit length. Here, the compressors are adding multiple bits which have same bit length and add the inputs of different bit lengths.

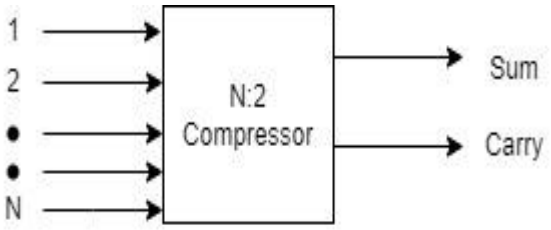


Figure 1: N: 2 Compressors

2.1 4:2 COMPRESSOR USING FULL ADDERS

The basic 4:2 compressor consists of 4 inputs and it gives only two outputs known as sum and carry bit along with these input and output pins one more input pin is added to the compressor called as carry in and it gives one more output called are carry out. The carry out generated from the compressor is propagated to the next bit positions. Hence these compressors generally have multiple input and multiple outputs.

$$X_1+X_2+X_3+X_4+C_{IN}= Sum+2*(Carry + C_{in}) \quad (1)$$

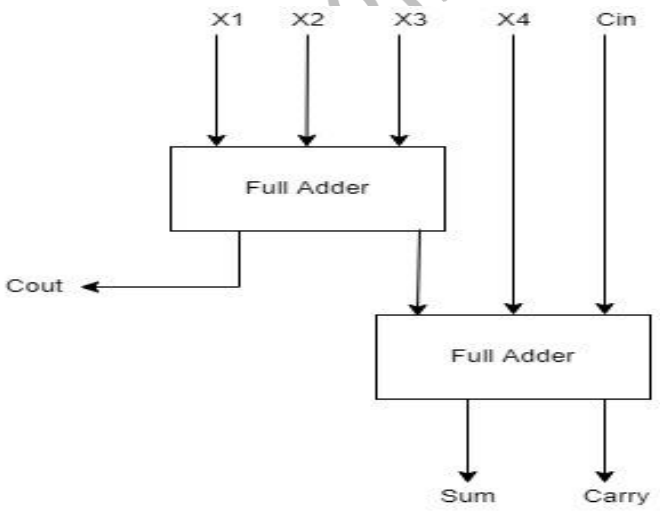


Figure 2: Conventional 4:2 Compressor.

2.2 CONVENTIONAL IMPLEMENTATION OF 3:2 COMPRESSOR

In general the 3:2 compressors are designed with the help of full adders and these compressors are the exact compressors. In the approximate compressors approximate computing is used and approximate full adders are designed and these approximate full adders are used to construct the approximate compressors. In the proposed higher order compressors instead of full adders XOR and MUX's are used to enhance the performance of the compressor. With the use of these proposed compressors power consumption and delay are gradually reduced. The conventional compressor using XOR and MUX is shown in the figure 3.

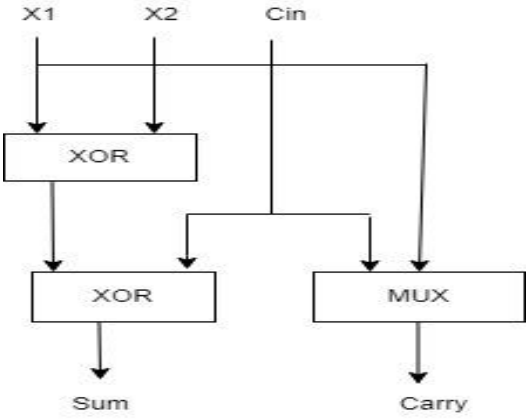


Figure 3: Conventional implementation of 3:2 compressor

2.3 4:2 COMPRESSOR BASED ON XOR- MUX ARCHITECTURE

With the same approach for 4:2 compressor has been designed as below. The 4:2 compressors are the basic compressor used in designing every multiplier. The proposed design is implemented with the XOR gates and multiplexers to reduce the delay and power consumption.

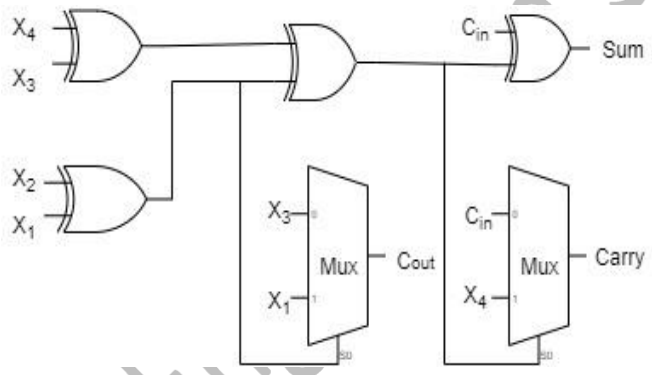


Figure 4: 4:2 Compressor based on XOR- MUX

The sum output of the compressor is evaluated as XOR inputs and C_{out} is calculated by multiplexer which selects the one input based on the XOR output of first two inputs. The sum equations is given in equation (2) and carry equation is given in equation (3).

$$Sum = a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7 \oplus C_{io} \oplus C_{i1} \oplus C_{i2} \oplus C_{i3} \oplus C_{i4} \quad (2)$$

$$Carry = ab + bc + ca \quad (3)$$

2.4 10:2 COMPRESSOR

With the use of approximate computing there is an occurrence of error is very high due to the reduction of the carry bits. Hence the lower order compressors are consuming high power although they are producing error outputs. Hence the higher order compressors are designed with the use of multiplexers and XOR gates due to these the power consumption for calculation is also gets reduced. The 10-2 compressor is having only 10 inputs and it gives only 2 outputs. This compressor has fourteen XOR gates and six multiplexers. Each XOR gate receives two primary inputs and it generates single output. Outputs of the XOR gates are propagating to the multiplexers in which the final multiplexer will generate the carry bit and the final XOR gate generate the sum output.

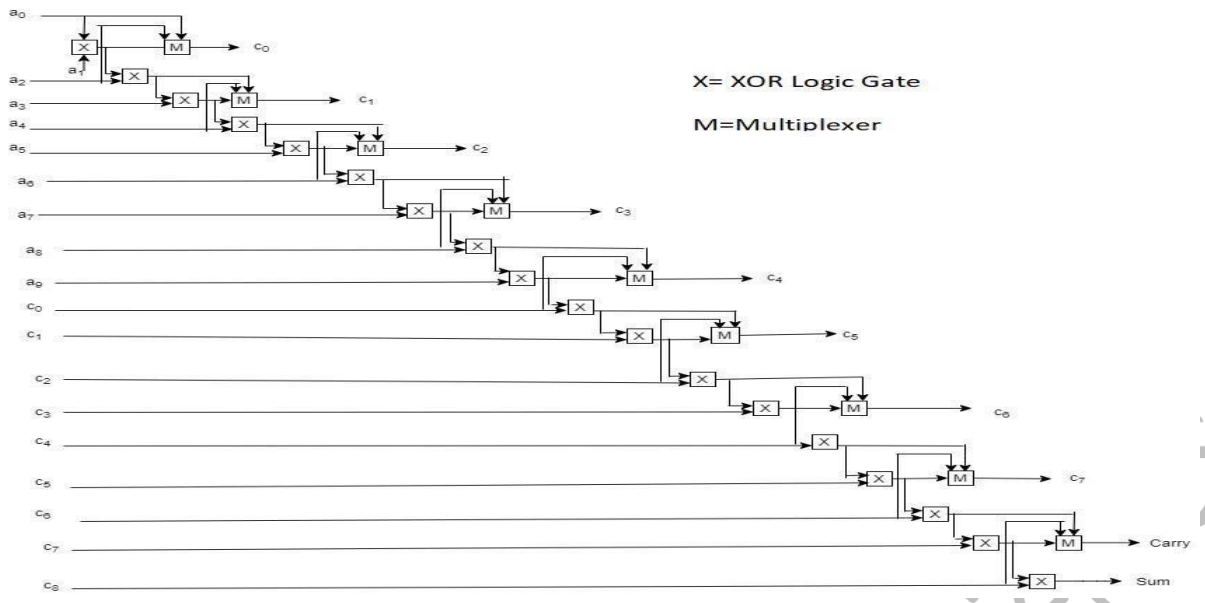


Figure 5: proposed 10:2 compressor based on XOR- MUX modules

3. DESIGN OF 32-BIT APPROXIMATE MULTIPLIER

The proposed 32 × 32 multiplier is represented in this paper. Along with 10:2 compressors other approximate compressor like 8:2, 4:2 and approximate half adder and approximate compressors are used for partial product reduction. The approximate 32-bit approximate multiplier consists of the proposed 10:2 compressors. Here 10:2 compressor is implemented using XOR and MUX modules only, with the use of XOR logic gates the power consumption of the design is getting reduced. Multiplexers are used in carry selection mechanism in which carry bit with higher logic is neglected which means it will not propagate to next level thus reducing the carry circuity resulting in decrease of delay output. The proposed 32 bit multiplier generates 1024 partial products. These partial products are reduced using proposed 10:2 compressor and other approximate lower order compressor which results in 3 stages of reduction.

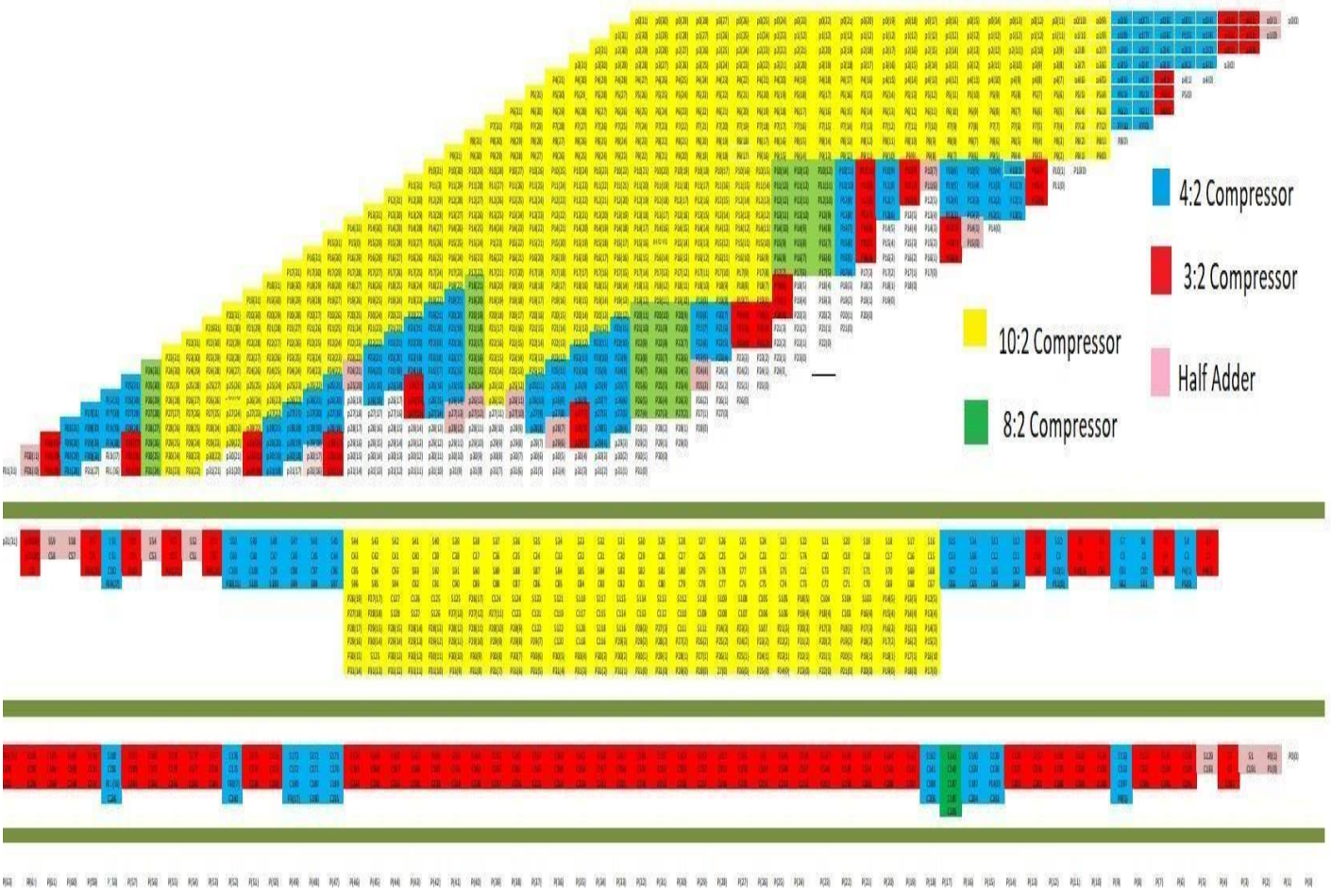


Figure 7: Internal Architecture of Proposed 32-bit Approximate Multiplier with Reduction Stage.

3.1 SIMULATION RESULTS

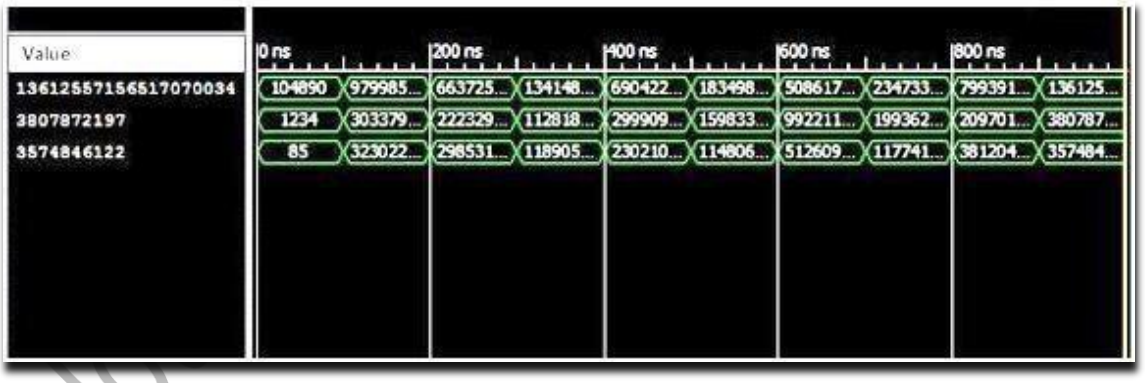


Figure 8: Simulation result of the 32-bit Exact multiplier

Figure 8 represents the simulation result of the 32 bit exact multiplier. Two input values are considered for exact multiplication and the output value is calculated. The exact multiplication is performed on set of data that is represented in timing diagram.

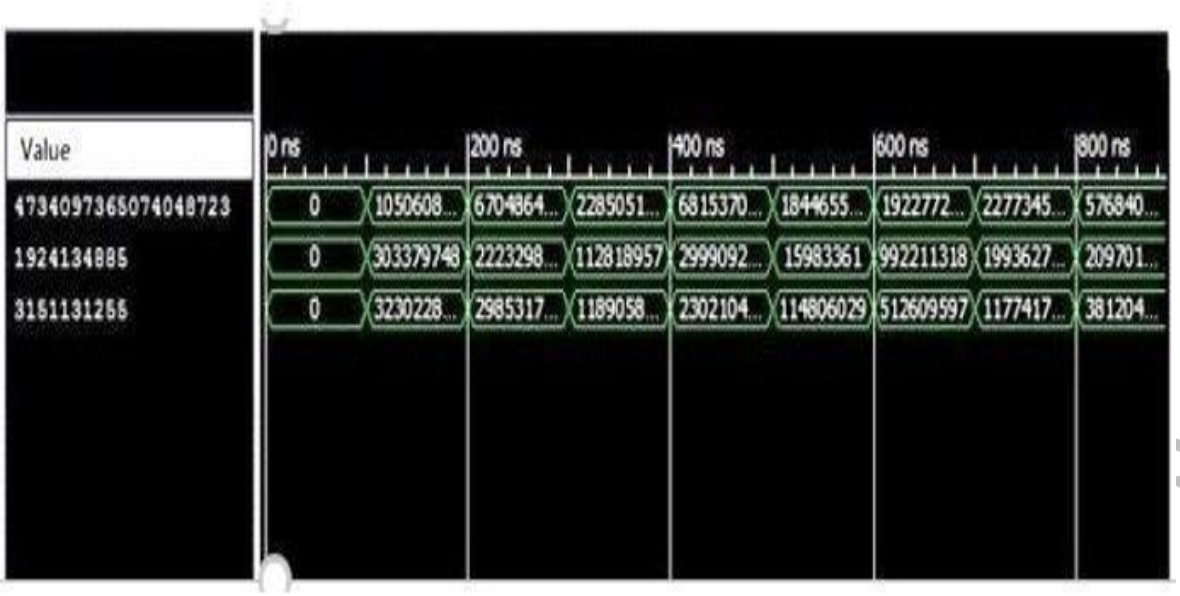


Figure 9: Simulation result of proposed 32-bit Approximate Multiplier.

Figure 9 represents the simulation result of the 32-bit approximate multiplier. Two input values are considered for the approximate multiplication and the approximate output is calculated. The approximate multiplication is performed on set of data that is represented in Timing diagram.

Table 1: Comparison of 8, 16 and 32-bit exact and approximate multipliers

Multiplier	Delay(ns)	LUT count
Exact 8 bit	7.664	124
Approximate 8 bit	2.969	84
Exact 16 bit	12.007	551
Approximate 16 bit	4.689	242
Exact 32 bit	20.55	2255
Approximate 32 bit	18.898	1705

4. IMPLIMENTATION OF FIR FILTER AND IMAGE PROCESSING APPLICATION USING PROPOSED 32-BIT MULTIPLIER

Higher order compressors play a vital role in realizing high speed multiplier. In this project work a new implementation method for 10:2 compressor based on XOR- MUX modules are used to design 32-bit multiplier. This approximate 32-bit multiplier is used to design a FIR filter. The proposed multiplier has reduced the delay of FIR filter to a great extent.

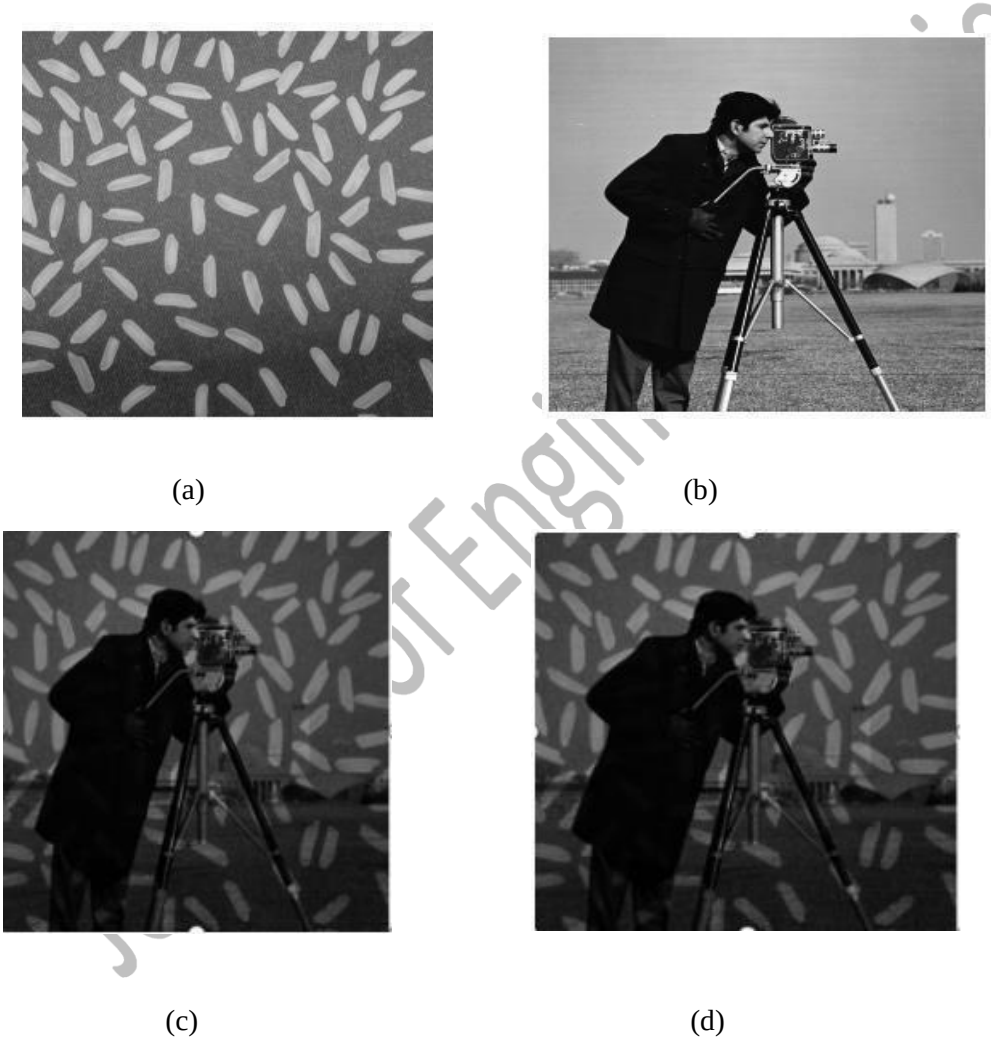
Filter	Delay (ns)
Accurate	119
Approximate	27

Vol 13, Issue 06, June/2022

ISSN NO:0377-9254

4.1 IMAGE PROCESSING APPLICATION

At present, image processing plays a vital role for the transmission of data. Here the data is transmitted in the form of images and these images are the combination of pixels. The image quality and accuracy is completely depends on the pixels. The images are transmitted with the multiplication of multiple images. In this paper combination of two signals shows that the image quality and precision. For the combination of two image different multiplication techniques are implemented among them the approximate multipliers gives the better results without any loss of the image pixels. Hence in this paper, the proposed multiplier is used for the combination of two images which gives the better PSNR compared with the previous multiplication techniques. While the transmission of images are digital the digital images consists of a finite number of elements.



(a) (b)

(c) (d)

Fig. 11 a) First input image that is considered for multiplication b) Second input image that is considered for multiplication. c) output image obtained by multiplying images using exact 32-bit multiplier d) output image obtained by multiplying using our proposed approximate 32-bit multiplier.

Multiplier	PSNR (db)	SNR
Exact	18.4167	6.4595
Approximate	23.1856	9.2284

PSNR value of resulted image in exact multiplication is 18.4167 db whereas in proposed approximate multiplication we got 23.1856db which is better than exact multiplication.

5. CONCLUSION

Approximate 32 × 32 bit multipliers are designed using the proposed 10-2 compressor. The proposed multiplier is used for implementing FIR filter resulted 27ns delay which is far better than the exact multiplier having 119 ns delay output. This approximate multiplier is used to multiply different images and PSNR value is evaluated. Using approximate multiplier, we got PSNR value of resulted image as 23.1856 db where as in exact multiplier PSNR value is 18.41 db. The proposed multiplier achieves better PSNR values with the previous designs. Finally, our proposed multipliers show high speed when compared to exact multipliers.

REFERENCES:

[1] M. Maria Dominic Savio and T. Deepa, "Design of Higher Order Multiplier Approximate Compressor" © 2020 IEEE.

[2] Che-WeiTung and Shih-hus Huan, "Low Power High Accuracy Approximate Multiplier Using Approximate High Order Compressor" 2019 2nd International Conference on Communication Engineering and Technology © 2019 IEEE.

[3] Chip-hong Chang, JiangminGu and MingyanZhang, "ultra-Low Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits", IEEE Transactions on Circuits and systems: Regular paper, vol.51, pp.1985-1996, October 2004.

[4] Mahnoush Rouholamini, Omid Kavehie, Amir-pasha Mirbaha, SomayeJafaraliJasbi and KeivanNavi, "A New Design of 7:2 Compressor", IEEE International Conference on Computer systems and Applications.

[5] Surekha, N. Porselvi and Kumutha Priya .K, "An Efficient High Speed Wallace tree multiplier", IEEE International Conference on Information Communication and Embedded systems,2010@ IEEE.

[6] SK Anusha, M. Krupa Swaroopa Rani, "Design and Implementation of Inexact Compressors by using multiplication", International Journal of Innovative Technology and exploring Engineering, volume 8, Issue-9, 2019.

[7] Karri Manikanta Reddy, M. H, Vasantha, Y.B. Nithin Kumar and Devesh Dwivedi, "Design and analysis of multiplier using Approximate 4:2 compressor", International journal of Electronics and communication.

[8] Marimutu R, Elsie Rezinold Y and P. S Mallick, "Design and Analysis of Multiplier Using Approximate 15:4 Compressor", 2016@ IEEE.

[9] A. Momeni, J. Han, P. Montuschi and F. Lombardi, "Design and Analysis of Approximate Compressor for Multiplication", IEEE Transactions on Computers, 2013.

[10] Guo, Y. Sun, Guo, and Kimuara, "Low-cost Approximate Multiplier Design using Probability-driven inexact Compressor", Asia Pacific Conference on Circuits and Systems, pp:291-294,2018, IEEE.

[11] Prasnose J. Edaroor, Sithere Raveendran and Amol D. Rahulkar, "Approximate Multiplier design using Novel Dual-Stage 4:2 Compressor", Science and Engineering Research board, Volume-8, 2020, IEEE.

[12] Suganthi Venkata Chalam and Seok-Bum Ko, "Design of Power and Area Efficient Approximate Multipliers", IEEE Transactions on VLSI, pp: 1063-8210© 2015 IEEE.

[13] Manjunath, Venama Harikiran, Kopparapu Manikanta and Sivasankaran K, "Design and implementation of 16-bit Modified Booth Multiplier", International Conference on Green Engineering and technologies,2015, IEEE.

[14] E. Jagadeeswara Rao, K. Jayaram Kumar and Dr. T. V. Prasad, "Design of High-Speed Wallace tree Multiplier using 8:2 and 4:2 adder Compressor", International Journal of Engineering and technology, Volume 7, Issue-4, pp:2386-2890,2008.

[15] Sreehari Veeramachaneni, Kirthi Krishna M, Lingamaneni Avinash and Sreekanth Reddy Puppala. "Novel Architecture for High-Speed and Low-Power 3:2, 4:2, and 5:2 Compressors", 20th International Conference on VLSI design, © 2007 IEEE.

[16] M. Abheesh Kumar, A. Sudhakar and J. Venkata Suman, "Design and Implementation of Compressor based 32-bit multipliers for MAC Architecture", IJITEE,2019.

[17] S. Srikanth and G. Vishnu Priya, "Low power Array Multiplier Using Modified Full adder", 2nd IEEE conference on Engineering and Technology© 2016 IEEE.

[18] Aishwarya Raj and T. E. Ayoob Khan "A 4-bit Dadda Multiplier with Full Swing output adders", AIP conference, 2020.

[19] Jyothi kamatam and Kumara swamy Gajula, "Design of Array Multiplier Using MUX based full adder", International Journal of Engineering Research and Technology, Volume 6, Issue 5,2017.

[20] Muhammad Hussain Riaz and syed Adrees Ahmed, "Low power 4-bit Multiplier Design and Dadda Algorithm and Optimized Full adder", 15th International Bhurban Conference on applied Science and Technology,2018.