JES
Journal of Engineering Sciences

Vol 13, Issue 06, JUNE/2022

ISSN NO:0377-9254

# A HIGH SPEED WALLACE TREE ENCODER USING HYDRID FULL ADDER

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ABSTRACT: Power consumption of analog and digital circuit design is will play major role in the world. Many researchers involved in designing the low power analog and digital circuits. The nature of signal is generated in real time is analog. Nowadays signal analyzes is done in digital for only to achieve low power, high accuracy, speed and less area. In the work, the VLSI architecture design for Wallace tree encoder with modified full adder is proposed. In analog to digital conversion process, Wallace tree encoder is utilized in the process of converting the thermometer code to binary. This can be termed to be a high speed application and a flash type of flash ADC, which is a resistor ladder, encoder and comparator circuit. A suitable encoder is required for getting binary code from comparator output. Reducing energy of the encoder is a vital concern whereas designing the minimal power flash form ADC. Wallace tree encoders diminishes the mistake due to the availability of zeroes in the sequence of the once presence to the series of zeroes in a comparator output, but it consumes more power. Hence in the proposed work, a low power Wallace tree encoder is designed using pass transistor logic (PTL) full adder.

## 1. INTRODUCTION

Power consumption of analog and digital circuit design is will play major role in the world. Many researchers involved in designing the low power analog and digital circuits. The nature of signal is generated in real time is analog. Nowadays signal analyzes is done in digital for only to achieve low power, high accuracy, speed and less area. So, the conversion of Analog to Digital is very important and also it is implemented in all real time signals processing analysis. The conventional analog to digital converter will consume more power. Some of the ADC developed in the last decade . High speed traditional to modernized converters is formulated and evaluated.

A parallel structure of flash ADC will reduce the delay of the ADC when compared with conventional ADC[6]. Various low powers Wallace tree multipliers are designed [7]. Each reference voltage is connected to comparators in the architecture. The comparator compares and produces the output in the type of modern 0's and 1's when reference ladder generates the reference voltage. Then the binary value is converted into thermo code. The binary conversion is done by Wallace Tree encoder utilizing bubble error logic [8]. To synchronize the binary values each output comparator output is to make high conversion. Area, power increases and component number enhances exponentially. In order to generate a reference voltage for the 2N -1 comparators are required N-bit

flash ADC 2N resistors. Thermometer code is nothing but the collection of comparator output. In order to change the code of thermometer to the code of binary is with the assistance of the simplified 2N - 1: N encoder.

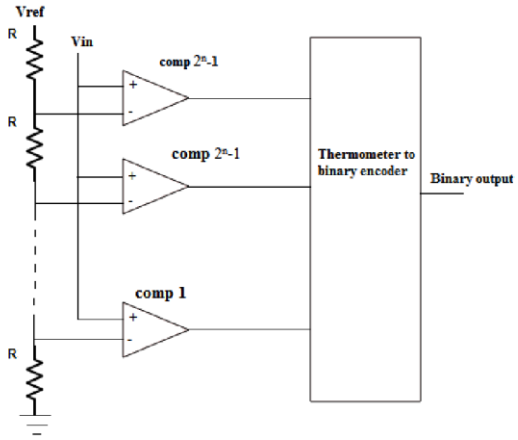



Fig. 1: Basic block diagram of flash ADC

While the design of the flash analog to digital converter, need to consider the speed, area and power. They introduced the Wallace tree counter that counts the 1's availed to the comparator [9]. Bubble errors can dealt with by higher input NAND gates and used to design the fat tree encoder and ROM encoder [10, 11]. More power consumption is the bottleneck of this work.

Full adder will play major obligation in the Wallace design tree encoders. The 2N – N – 1 bit of adder is utilized to design encoder. The conventional full adder of the Wallace tree encoder shall influence the general performance of the framework. Requires an optimization the full adder to get the better performance of the Wallace tree encoder. In this paper, the proposed work is concentrated on power reduction by replacing conventional full adder by modified hybrid full adder thereby to achieve power reduction.

## 2. LITERATURE SURVEY

Highly-digital voltage scalable 4-bit flash ADC by Ashima Gupta1, Anil Singh1, Alpana Agarwal

This study describes the highly-digital 4-bit 200 MS flash analogue to digital converter (ADC) whose major part can be digitally synthesized thus achieving low power, reducing the time-to-market and is scalable with technology. The comparators used in the ADC consist of complementary metal–oxide–semiconductor (CMOS)-based inverter and NAND-NOR as standard cells. The complete flash ADC is designed in 180 nm CMOS technology with 1.8 V supply with the power consumption of 4.51 mW. The signal-to-noise and distortion ratio, signal-to-noise ratio and spurious-free dynamic range are equal to 23.3, 25.2 and 30.1 dB. It provides an effective number of bits equal to 3.5. The differential non-linearity (DNL) of this ADC is ± 0.25 LSB and integral non-linearity (INL) is + 0.6 LSB.

Cmos Full Adder and Multiplexer Based Encoder for Low Resolution Flash ADC by M.Kiranmai, V.Y.S.S.Sudir patnaikuni, K.Mouli, B.Manikanta sai, V. Nancharaiah

The present investigation proposed a low power encoding scheme of thermometer code to binary code converter for flash analog to digital conversion by the design of different circuits. In this paper, we have proposed three encoding techniques for the conversion of analog to digital signal using Multiplexer based encoder, heterogeneous encoder and encoding technique using dynamic logic circuits providing low power of operation and we compare the results obtained from each technique based on power consumption. The multiplexer based encoder was designed with the help of multiplexers which consumes less amount of power comparing with other designs.

A Survey on Different Modules of Low-Power HighSpeed Hybrid Full Adder Circuits by Vivek Saraswat, Ankur Kumar,

In this paper, a review study and analysis of designs for 1-bit hybrid full adder is demonstrated. The hybrid full adder is decomposed into three sub-modules. For each sub-module, different designs are simulated and analyzed. Each module exhibits different speed, power consumption and area. Ten different 1-bit hybrid full-adder cells are created by combining possible arrangements of different designs of sub-modules. Each of these hybrid full adder cell differs from one another in terms of transistor count, average power dissipation and delay. All the circuits have been designed using CADENCE Virtuoso tool at 45-nm technology and simulation is done using SPECTRE simulator. Comparison of performance parameter like power dissipation and delay is done with the existing standard adder cells transmission gate adder, complementary pass-transistor logic (CPL), and conventional CMOS adder.
Design and implementation of a novel flash ADC for ultra wide band applications by Varghese, G.T.:
This dissertation presents a design and implementation of a novel flash ADC architecture for ultra wide band applications. The advancement in wireless technology takes us in to a world without wires. Most of the wireless communication systems use digital signal processing to transmit as well as receive the information. The real world signals are analog. Due to the processing complexity of the analog signal, it is converted to digital form so that processing becomes easier. The development in the digital signal processor field is rapid due to the advancement in the integrated circuit technology over the last decade. Therefore, analog-to -digital converter acts as an interface in between analog signal and digital signal processing systems. The continuous speed enhancement of the wireless communication systems brings out huge demands in speed and power specifications of high-speed low-resolution analog-to -digital converters. Even though wired technology is a primary mode of communication, the quality and efficiency of the wireless technology allows us to apply to biomedical applications, in home services and even to radar applications. These applications are highly relying on wireless technology to send and receive information at high speed with great accuracy. Ultra Wideband (UWB) technology is the best method to these applications. A UWB signal has a bandwidth of minimum 500MHz or a fractional bandwidth of 25 percentage of its centre frequency. The two different technology standards that are used in UWB are multiband orthogonal frequency division multiplexing ultra wideband technology (MB-OFDM) and carrier free direct sequence ultra wideband technology (DS-UWB). ADC is the core of any UWB receiver. Generally a high speed flash ADC is used in DS-UWB receiver. Two different flash ADC architectures are proposed in this thesis for DS-UWB applications. The first design is a high speed five bit flash ADC architecture with a sampling rate of 5 GS/s. The design is verified using CADENCE tool with CMOS 90 nm technology. The total power dissipation of the ADC is 8.381 mW from power supply of 1.2 V. The die area of the proposed flash ADC is 186 μm × 210 μm (0.039 mm2). The proposed flash ADC is analysed and compared with other papers in the literature having same resolution and it is concluded that it has the highest speed of operation with medium power dissipation. iii The second design is a reconfigurable five bit flash ADC architecture with a sampling rate of 1.25 GS/s. The design is verified using CADENCE tool with UMC 180 nm technology. The total power dissipation of the ADC is 11.71 mW from power supply of 1.8 V. The die area of the implementation is 432 μm × 720 μm (0.31104 mm2). The chip

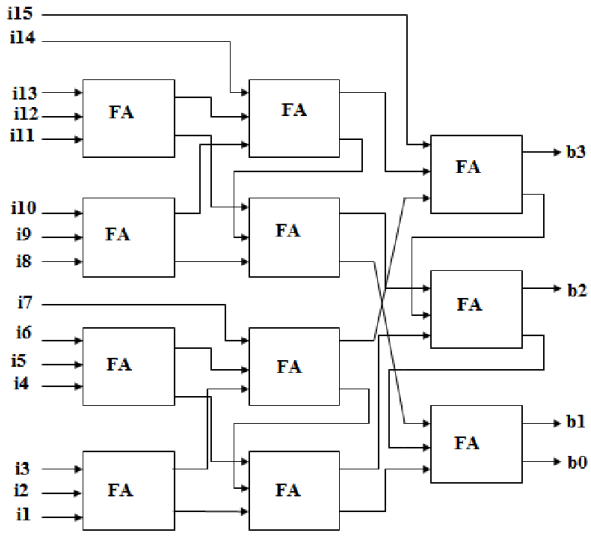
tape out of the proposed reconfigurable flash ADC is made for fabrication.

Design and implementation of a 5-bit flash ADC for education by Abualsaud, A.A., Qaisar, S., Ba-Abdullah, S.H.,

The DSP (Digital Signal Processing) has many advantages over the analog processing. Therefore, with the recent advent of technology most of the signal processing tasks have been transferred from the analog to the digital domain. The ADCs (Analog to Digital Converter) provide a liaison between the real world analog signals and the digital processors. Therefore, ADCs become an elementary part of almost all modern electronic systems. This work focuses on the development of a simple Flash ADC for students demonstration purpose. In this context, a 5-Bit Flash ADC is implemented. Being designed for illustration purpose, the ADC has easily accessible inputs and outputs to each module. In order to keep the system cost effective with an ease of reimplementation. The low cost and easily market available discrete analog components are employed. The digital part is kept configurable with the help of a FPGA (Field Programmable Gate Array) based implementation. The digital circuit implementation is done via Verilog, a HDL (Hardware Description Language). The system implementation is described. Testing results are also presented. These results assure a proper functionality of the designed ADC

## 3. EXISTING SYSTEM

It consists of eleven full adders with 15 thermometer code inputs and four binary outputs labeled as b3, b2, b1, b0. In the existing type of Wallace tree encoder, all the 15 inputs starting from i1 to i15 are channeling via equal number of complete adder. Hence the propagation delays between each input and the corresponding output is effectively controlled and also identical [13]. So speed of operation of the existing design is reasonably good. In this design conventional full adder is used and each of the full adders consists of 28 transistors. Totally 308 transistors are required for full adder Wallace design tree encoder and hence the prevailing circuit takes up more energy.

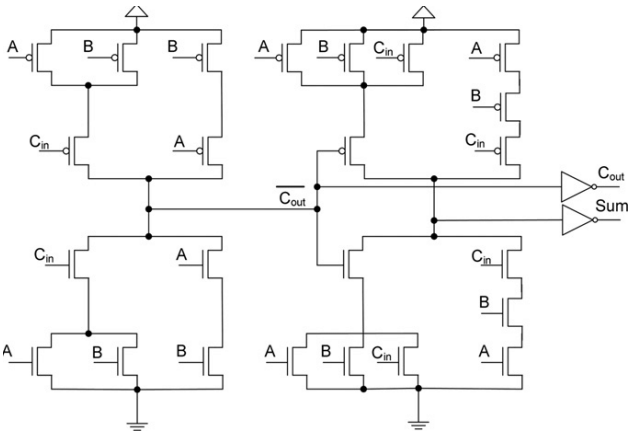



Circuit realization for low power and low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. The full adder circuit adds three one-bit binary numbers (Cin, A, B) and outputs two one-bit binary numbers, a sum (SUM) and a carry (COUT). Due to the important role played by Full adder in various arithmetic units, optimized design of Full adder to achieve low power, small size and delay is needed. The primary concern to design Full adder is to obtain low power consumption and delay in critical path and full output swing with low number of transistors to implement it

A basic Full adder cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (sum and carry). The relations between the inputs and the outputs are expressed as:

SUM = A ⊕ (B ⊕ C)

COUT = AB + BC + AC




The above shown Conventional full adder [1] is a combination of PMOS pull up transistor and NMOS pull down transistor. It is well known for its robustness and scalability at low supply voltages. But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

## 4.PROPOSED SYSTEM

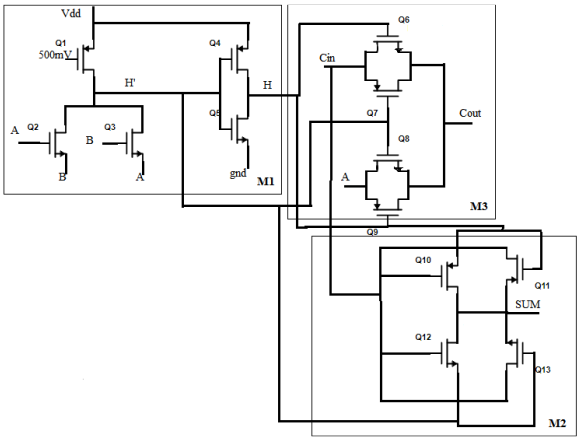
The major purpose of the recommended research is to formulate the minimal energy, less optimal speed and minimal complexity Wallace tree encoder that is used in both the traditional and modern conversion procedure. In the recommended design energy consumption of the Wallace tree encoder that is diminished by the corrected design of the complete adder. The adapted complete adder comprises of about 13 transistors. By reducing the number of the transistors, the energy consumption of the complete adder can be reduced.

The proposed full adder design employs only 14 transistors as shown in Fig. 1. It mainly consists of five logic blocks designed using technique. One XOR/XNOR, two multiplexer's, one Swing Restored Transmission Gate (SRTG), and the other one is Swing Restored Pass Transistor (SRPT) block. The XOR/XNOR block is designed using GDI technique. Since the path of the inverters used in the XOR/XNOR blocks has no voltage drop, they are incorporated with standard *VT* devices. Since the GDI MUX-1, multiplexes the output of the XOR (A AXOR B) and the XNOR (A XNOR B) with a control input (*C*in) to obtain the sum function. Therefore, the (3) can also be represented as in (5).

$$\text{Sum} = \overline{C_{in}}(A \oplus B) + C_{in}(A \odot B) \quad (5)$$

The carry output (*C*out) is generated by the GDI MUX-2, which multiplexes the inputs *C*in and B with control line from the output of XNOR logic (A XNOR B). Therefore, the (4) can also be represented as in (6).

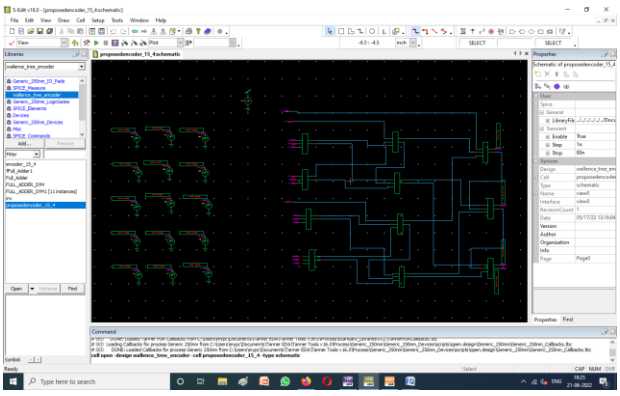
$$C_{out} = \overline{(A \odot B)}C_{in} + (A \odot B)B \quad (6)$$

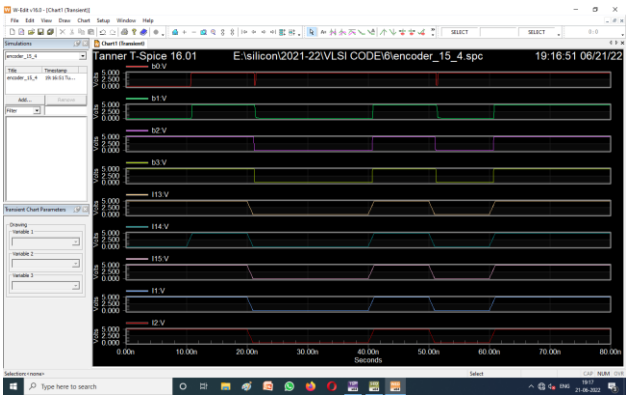



However, the proposed structure looks similar to many previous XOR/XNOR logic-based designs and authors' previous design, but none of the previous designs provides full logic swing with only 14 transistors. In the proposed design, the full swing is ensured using a SRTG at the output of the sum and SRPT's at the carry output (*C*out). It can be observed that the swing restoration transistors (M11, M12, M13, M14) are 'ON' when there is a *VT* drop at the output of the sum generation MUX1 and *C*out generation MUX-2 to provide full swing logic. Since there is no *VT* drop at the

output in most of the cases as stated in Table 4, the transistors (M11, M12, M13, M14) are also incorporated with standard *VT* transistors.

## 5. RESULTS






## 6.COMPARISION TABLE

| EXISTING SYSTEM | PROPOSED SYSTEM |
|---|---|
| •For one full adder 28 transistors required | •For one full adder 13 transistors required |
| •Total transistors are 308 | •Total transistors are 143 |
| •Circuit complexity is more | •Circuit complexity is less |
| •More power consumption | •Less power consumption |
| •More time delay | •Less time delay |

## 7. CONCLUSION

The proposed work describes low power, less complexity and optimum delay Wallace Tree encoder by suitable design of full adder. It dissipates power 74.15nW with delay 0.0495ns. The projected is formulated based on the application of the Tanner EDA program, which is simulated based on the application of the tspice.

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