FPGA Based Performance Comparison of Different Basic Adder Topologies with Parallel Processing-64bit

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Abstract: Now a days in the world of VLSI Technology, the word low power consumption is only possible with the concept of Reversible logic design. Reversible concepts will attain more attraction of researchers in the past two decades, mainly due to low-power dissipation and high reliability. It has received great importance due to because of there is no loss of information, while we are processing the data from input to output. The study of designing fast circuits that use less power and take up less space is one of the most important aspects of VLSI design. One of the most common digital circuit components is the adder. Compared to other fast adders, this is one of the most compact and energy-efficient. This study proposed a 64-bit carry choose adder employing a modified XOR-based full adder to minimize circuit complexity, size, and latency. Only two XOR gates and a single multiplexer are needed in the improved complete adder. In terms of size, power consumption, and latency, the modified 32-bit carry-select adder is superior than the standard carry-select adder.

Keywords: low power, area efficient, XOR based adder, carry select adder

1.0 INTRODUCTION

An adder is an element which performs addition of numbers. Adders are useful in arithmetic logical units (ALU) which are widely used in computers and different types of processors. For effective and efficient implementation of arithmetic components adders play an important role. Adders can be treated as building blocks of the arithmetic component. For the operations like complementing, decoding and encoding adders are used. Generally, addition involves adding of two numbers which generates sum and carry. All adder architectures either simple or complex are constructed by using fundamental blocks which are half adder and full adder. For small number of bits, simple adders like ripple carry adder, carry look ahead adders are sufficient. However, delay increases as the bits number increases because of the passing of the carry to the next stage. So we use Parallel Prefix Adders to perform arithmetic operations on large number of bits. Parallel prefix adders are high speed adders and takes small area and gives less delay. These adders consume low power and relatively takes less area on chip. Primary concern of adders is speed and later we have chip area and power consumption of adder.

Related Work:

There are some methods to mitigate or detect soft errors (SEs) in FPGAs. One of them is known as data scrubbing (DS) DS is the process of scanning all device memory in some time intervals to correct the detected errors. It requires storing the original configuration or part of the original configuration data to replace the corrupted frames. Even though every frame of the FPGA bitstream has error correction code (ECC) bits, it may not be enough since ECC codes are only capable of correcting a single bit or two adjacent bits in a frame. Apart from the ECC codes, the bitstream is also protected by cyclic redundancy check (CRC) codes; however, CRC codes are only beneficial for integrity checks and are not useful for any error correction operation Triple module redundancy (TMR), combined with a voter mechanism, is another well-known method to increase the reliability and detect SEs Although this method drastically improves the mean time to failure (MTTF), the area and the power consumption is increased threefold compared to the original design.

2.0 LITERATURE REVIEW

[1] Ananthakrishnan et.al (2019) the snake is an essential element in every modern area. In this digital age, everyone is working on miniaturization. The three main aspects of design, namely, area, power consumption and delay need to achieve optimal balance. Because helpers have been used as a key component of complex digital networks, increasing the performance of digital providers will accelerate the speed of binary operations in such complex zones.
[2] Apoorva Raghunandan et al. (2019) a good VLSI model is a design with small footprints and quick surgery. According to Moore's law, as the number of transistors in a chip increases, so does the overall chip area. In VLSI design, it is important to improve the Area and Delay parameters.
[3] Krishna Vamsi et al. (2018) proposed an effective insect repellent design, which uses a multiplexer-based multiplexer design rather than using a snake-bearing wound, but an improved enhancer Replace the ripplebearing snake for effective results. Using this improved snake can reduce power consumption and reduce gate delays. The proposed proposal is to carry and store oil from 8-bit to 64-bit. With today's digital technology system, which is the most widely used 64-bit format? Since ripple-carrying snakes are one of the most common types of auxiliaries used in many forms, there is a prolonged delay in propagation and consuming more area and energy
[4] Shilpa K.C.; et.al (2018) All modern processors, including microprocessors and digital signal processors, have an arithmetic logic unit (ALU). The computational performance of these modern processors depends on the success of the ALU. The serpent is the foundation stone of the ALU which performs arithmetic and logical work. Existing helpers (such as half helpers, full helpers, ripple converters, skip carry assistants and pre-loaders) cannot respond to improvement goals, so this paper offers four types of introductions.
In this article, [5] Nagaraja Revanna et al. (2019) discussed the design of ads implemented through memristor. Explains the memristor-based design for standard ad architectures (ripple-bearing adder, bearing adder, and corresponding prefinder adder). Compare area and waiting time. Surprisingly, the Radix-2 CLA has the same complexity as the parallel adder prefect. The results show that in the adjacent price adder, the Kogge-Stone design has the best metrics for latency and area.
[6] Basavoju Harish et al. (2019) in the field of Very Large-Scale Integration (VLSI) design; circuit summing is one of the most widely used data transmission architectures. With the advancement of VLSI technology, research is emerging to design low-speed, high-speed, small-area, or combination of two architectures.
[7] C. Selsi Aulvina et.al (2018) This article largely compares the impact of the difference between the effectiveness of the ripple bear adder (RCA) and the adderte-save-adder (BSA), and measures the reduction in conventional power consumption by lender collectors -money at low voltage. Increased the rate of deferral, and provided technology to improve the BSA's tolerance for change. And this article introduces the concept of so-called pipelines and the usual fundraising activities other than the reduction of power in snakes.

3.0 **IMPLEMENTATION OF 64-BIT ARITHMETIC ADDERS**

Kogge Stone Adder carry generation stage Every column stage produces both propagate as well as generate signals. Generate signals which are calculated in the final stage are made XOR with initially produced propagate and generate signals to produce sum. The advantage in Kogge-Stone adder is that it generates carry bits in O (log2 n) time delay complexity which made itself gives best performance in VLSI implemented circuits. KS has minimum fan-out with large area. It reduces the critical path to great extent so that increases it's performance in implementing to higher bit adders like 32-bit, 64-bit, and 128-bitComparing with Brent-Kung adder. KS takes greater area for implementing but it has lesser fan-out. Which makes wiring congestion of this adder is a problem.

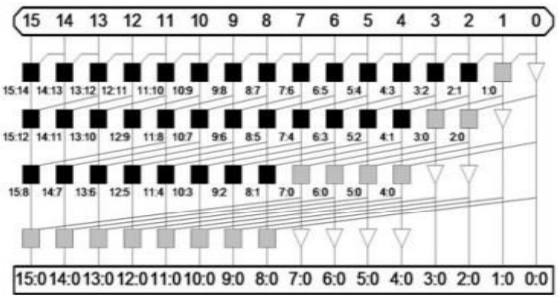

Fig 1: Kogge Stone Adder

Most digital circuits that perform addition or subtraction rely on a full adder circuit. It gets its name from the fact that it adds two binary digits plus a carry-in digit to produce a sum and a carry-out digit.

CRITICAL PATH:

DEFINITION: The critical path can be defined as the maximum delay path between the input and output.

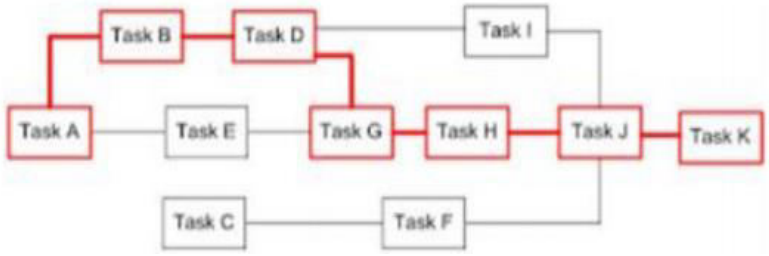

Fig 2: Critical path

Critical paths for different adders:

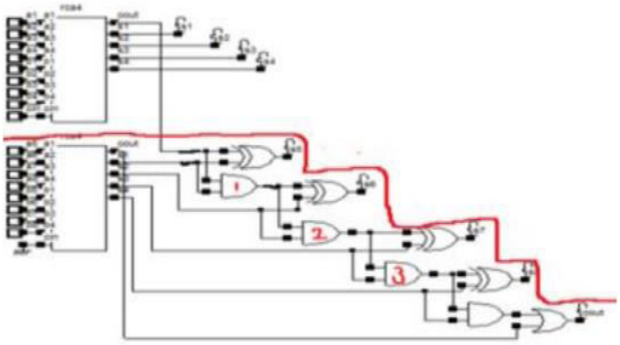

Fig 3: Critical path for 8- bit carry increment adder

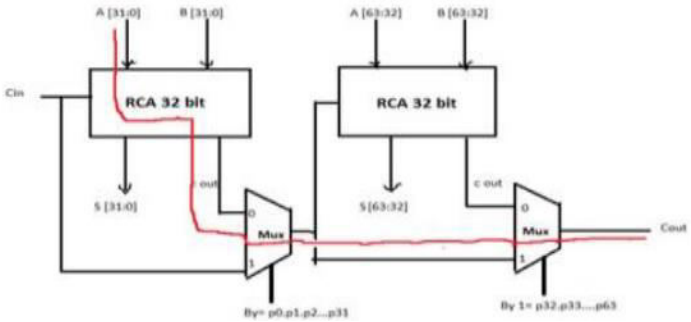

Fig 4: Critical path for 64-bit carry bypass adder

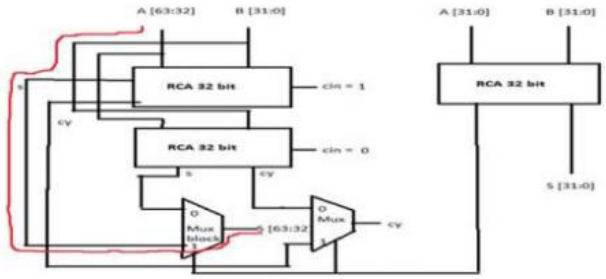

Fig 5: Critical path for 64- bit carry select adder

VLSI DESIGN:

To exponential advancement in convergence technology, large-scale systems architecture, the electronics sector has seen phenomenally development over the last two decades-briefly because of the VLSI introduction. There's been a

steadfast and very rapid increment in the amount and applications including integrated circuits in high-performance computing, telecom and electronic products. The needed processing capacity of these applications is usually the catalyst for the accelerated growth of this area, or in other terms the knowledge of such applications. Takes an analysis of the leading developments in IT in the next several decades. The new technology (including such low-bit video including wireless communication) provides end consumers with a certain amount of electricity and functionality in transmission.

FPGA: Users were able to incorporate preferred features for completely-fabricated FPGA chips through thousands or maybe more logic gates including programmable interconnections, including custom hardware programming. This style of design offers a means for rapid prototyping but cost-effective chip design, particularly for applications with low volume. The chip contains an I / O buffer, a collection of configurable logic blocks (CLBs), programmable connections architectures, and a standard Field Programming Gate Array (FPGA). Connectivity programming becomes achieved by the programming of RAM cells, which connect their output terminals to both the MOS passing gates.

Gate array design

Provided the rapid prototype features, the gate array (GA) approaches the FPGA. Whereas the FPGA chip is designed utilising user programming, the gate array is designed and processed using a metal mask. The very first phase, focused mostly on generic (standard) mask, results in either a selection of unconsumingtransists on even a GA chip. the very first phase entails a two-step processing process. This uncommitted chip could be deposited for later adaptation, which would be completed by specifying the metal connections here between array integrated circuits Because the metal interconnections are patterned only at end of chip output, the turning period may also be low, from a few days to a couple of weeks.

FPGA Design Flow Overview

The ISETM design flow includes the following steps: design input, design synthesis, design execution and programming of the Xilinx ® system. During design flow, design testing, which involves both practical verification and timing verification, takes place at numerous stages. This segment explains what you have to do for each phase. Click a box throughout Figure 5.5 for more information from each design phase.

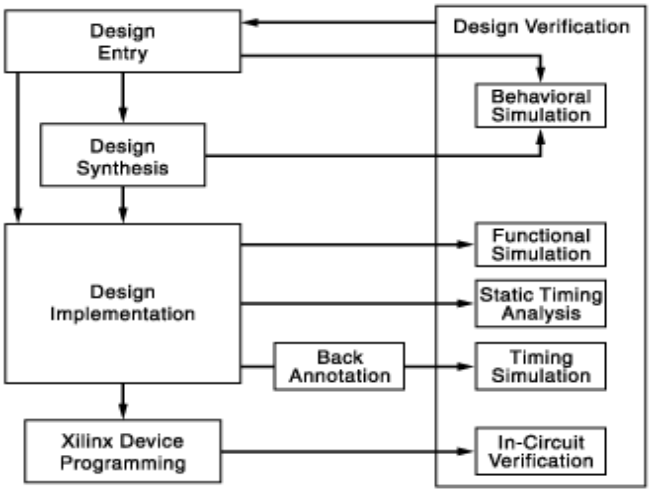

Fig 6: FPGA design flow overview

4.0 RESULTS

The proposed design methodology for 64-bit Carry select adder circuit with BEC has been synthesizedin XILINX program. The simulation results using Model sim simulator are shown in the figure

USING ISE DESIGN SUIT 14.4

Synthesis Tool: XST(VERILOG)

Simulator: ISim Simulator

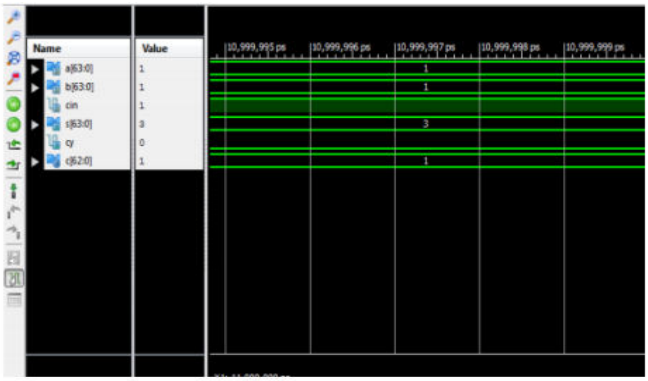

Fig 7: 64-bit ripple carry adder result

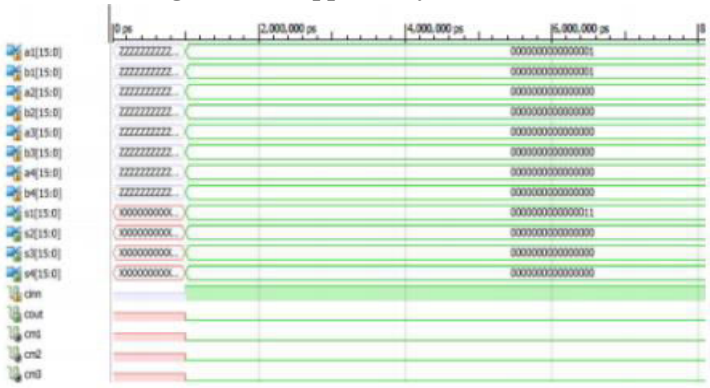

Fig 8: 64-bit carry lookahead adder result

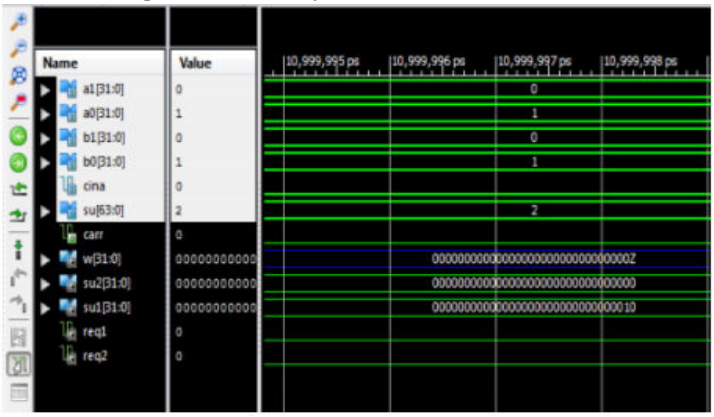

Fig 9: 64-bit carry increment adder result

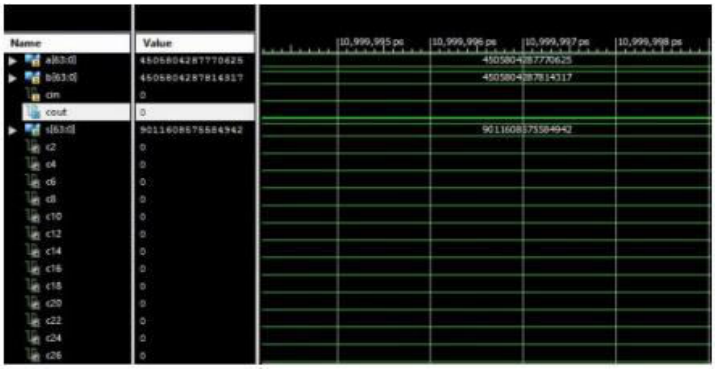

Fig 10: 64-bit carry skip adder result

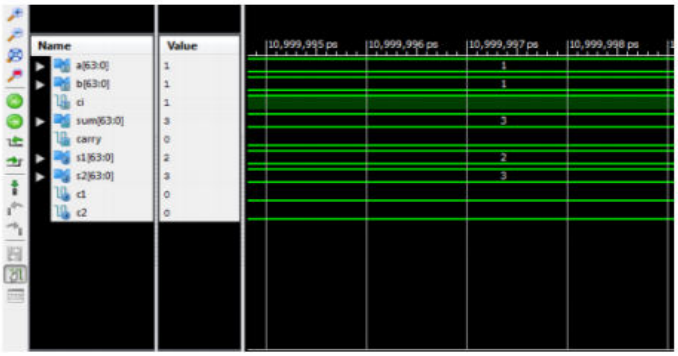

Fig 11: 64-bit carry select adder result

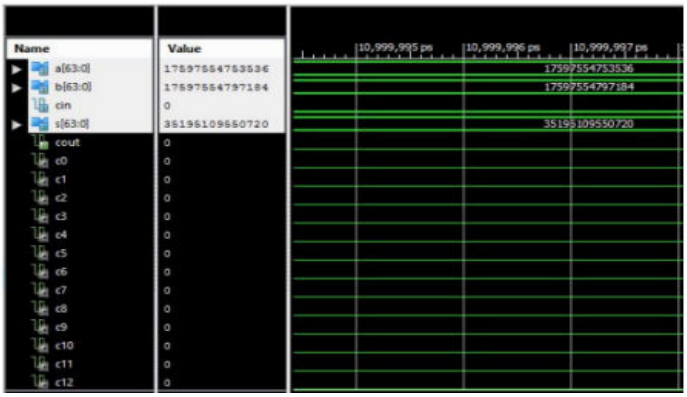

Fig 12: 64-bit Koggge stone adder result

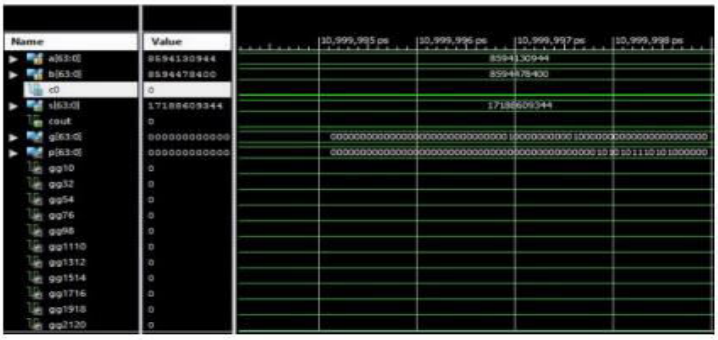

Fig 13: 64-bit Brent kung adder result

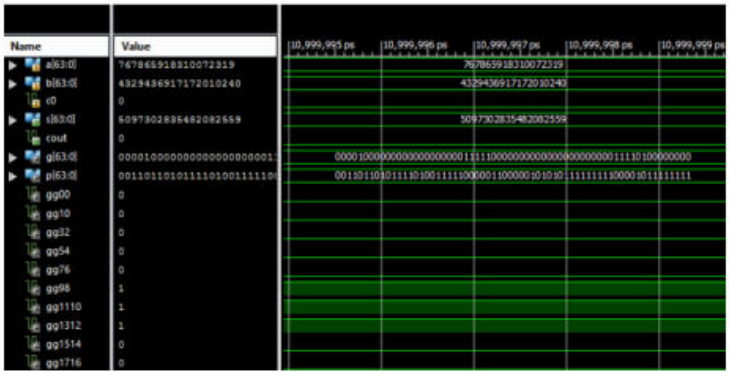

Fig 14: 64-bit Ladner fischer adder result

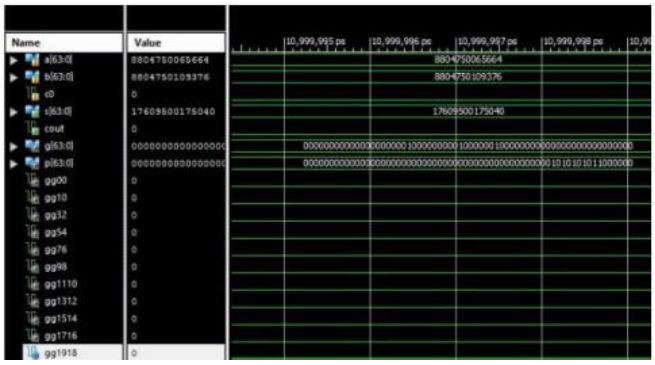

Fig 15: 64-bit Han carlson adder result

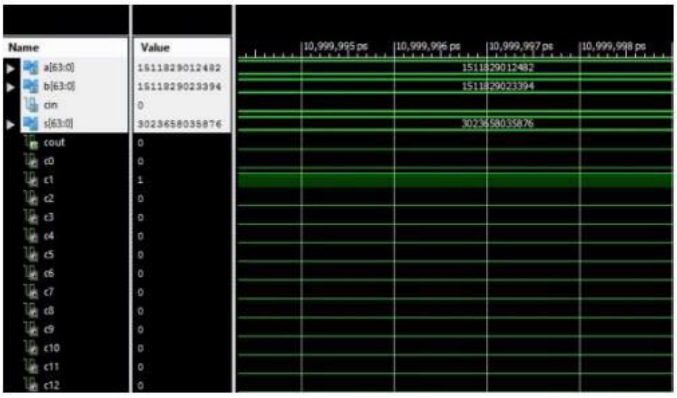

Fig 16: 64-bit Knowles adder result

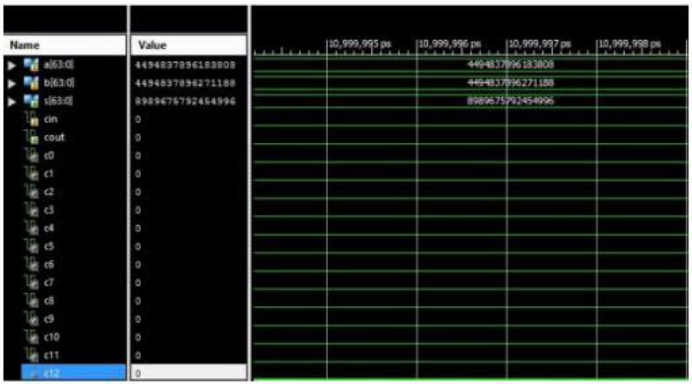

Fig 17: 64-bit Sklansky adder result

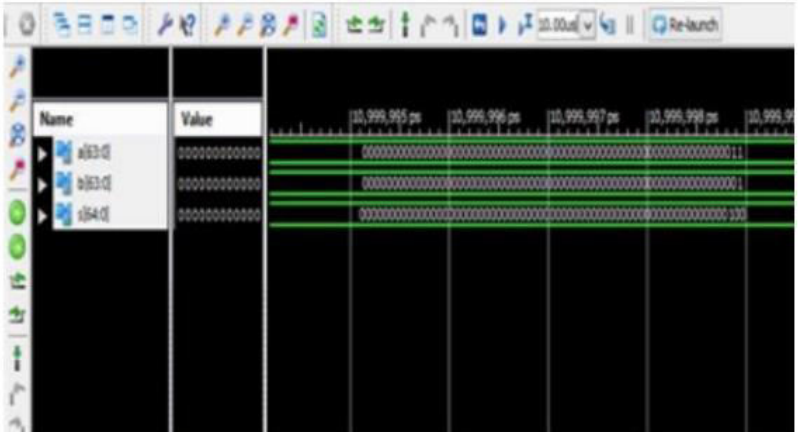

Fig 18: sum of two 64-bit numbers using XST

TABLE 1: DELAY COMPARISON OF ADDERS (64-BIT)

ADDER	DELAY(ns)
RIPPLE CARRY ADDER	95.75
CARRY LOOKAHEAD ADDER	37.12
CARRY INCREMENT ADDER	70.79
CARRY SKIP ADDER	92.12
CARRY BYPASS ADDER	57.85
BRENT KUNG ADDER	13.971
SKLANSKY ADDER	18.185
KOGGE STONE ADDER	28.526
LADNER FISCHER ADDER	21.029
KNOWLES ADDER	31.057
HANCARLSON ADDER	9.406
ADDER USING XST	10.049

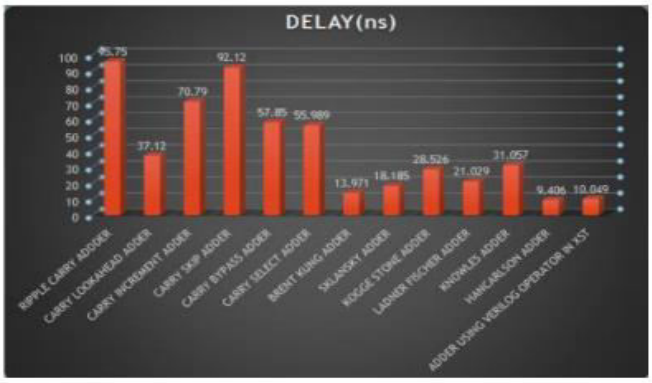

Fig 19: DELAY COMPARISON

DISCUSSIONS

The RTL view and simulation result using modified xor based carry select diagram is depicted the most disadvantage of convention Vedic multiplier is its major utilization According to the simulation results, an XOR-based 64-bit CSA consumes 20.40 percent less power, occupies 9.41 percent less space, and has a 2.01 percent shorter delay than a conventional CSA. The most significant disadvantage of the conventional al vedic multiplier is its extensive use of LUTs and slice registers; however, these issues are addressed.

CONCLUSION

Implementation of general-purpose DSP implementations often lacks the performance necessary for moderate sampling rates, and ASIC approaches are limited in flexibility and may not be cost effective. A Verilog implementation of FPGA based digital filters produces appreciable results because of various benefits like low power consumption, higher efficiency, faster etc.

From the delay comparison table Han Carlson Adder has least delay.

From the gate count comparison table Knowles adder has high circuit complexity.

- It's circuit complexity is in comparable with carry look ahead adder as we go for 64 bit addition.
- By using carry propagate adders we can get less delay for lower bit addition.
- As we go beyond that carry look ahead adder becomes more complex and requires high area. So we prefer parallel prefix adders at higher bit addition.
- For the addition up-to 64 bits we can get least delay by using HANCARLSON Adder.
- By taking gate count also into consideration Brent Kung adder is preferred.
- Han Carlson Adder got the comparable delay with the Adder using verilog operator in XST.

FUTURE WORK:

The designs can be further developed for higher bits. These designs can be implemented on FPGA and ASIC also. Also, by combining the different tree adders as well as the technology used to implement them, a suitable

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