IMPLEMENTATION OF MAJORITY LOGIC BASED COMPARATOR USING QUANTUM DATA CELLULAR AUTOMATA

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ABSTRACT

Quantum-dot cellular automata (QCA) logic is an advanced technology for developing the any combinational and sequential logics with less number of gates. Thus, in this work QCA technology was adapted to develop the combinational circuits like comparators and comparators of various sizes. Existing methods use the basic CMOS methodology to develop the comparators and comparators, but CMOS methodology failed to fulfill the lower area, delay and power consumption requirements as those designs requires more number of gates. Thus, the proposed approach utilizes QCA technique to implement comparator with less number of gates, these results in low area, power and delay consumption. Compared to the conventional methods, proposed QCA technique shows enhanced performance in area, delay and power consumption. The proposed comparator implemented using 18nm TSMC technology with Xilinx ISE software tool. Compared to the conventional methods, proposed QCA technique shows enhanced performance in area, delay and power consumption.

1. INTRODUCTION

Advancements in VLSI have been done on three variables: area and Delay, power. Area improvement implies decreasing the space of rationale which possess on the pass on. This is done in both front-end and back-finish of structure. In front-end structure, legitimate portrayal of rearranged Boolean articulation and expelling unused states will prompt limit the door/gate utilization. Segment, Floor arranging, Placement, and directing are act in back-finish of the plan which is finished by CAD tool[1].The CAD instrument have a particular calculation for each procedure to create a zone proficient structure like Power advancement. Force streamlining is to lessen the force dissemination of the plan which endures by working voltage, working recurrence, and exchanging movement. The initial two components are simply indicated in plan imperatives however exchanging action is a parameter which fluctuates powerfully, in light of the way which designs the rationale and information vectors. Delay improvement alludes to meeting the client imperatives in effective way with no infringement in any case, improving execution of the structure. QCA are an alluring rising innovation reasonable for the improvement

of ultra thick low-power superior advanced designs. QCA which utilizes exhibit of coupled quantum dabs to execute Boolean rationale work. The benefit of QCA lies in the incredibly high pressing densities conceivable because of the little size of the dabs, the rearranged interconnection, and the very low force defer item. An essential QCA cells comprises of four quantum specks in a square cluster coupled by burrow hindrances. Electrons can burrow between the specks, yet can't leave the cells. Comparator designs based on ML are existing in the literature. Very few architectures have the ability to implement all the three different functionalities of a comparator namely A>B, A and A=B. serial comparators are proposed using adiabatic pipelining. However, the approach in [4], offers the ability to extend it to implement n-bit comparator. Further, it achieves better reduction in majority gates (MG) compared to other existing designs. Parallel-prefix and tree architecture utilized in achieves high-speed designs. Priority encoding logic-based comparators [9, 10] can be a choice for high-speed dynamic logic but it failed to work for static logic. Dynamic double-tail comparator is applicable for low power low voltage requirements. Cross coupling mechanism is exploited in dynamic comparator to achieve low power high-speed operation. Dynamic bias comparators provides energy efficient biasing mechanism. This section provides a brief overview of [1] that contains four theorems (T1, T2, T3 and T4) and two corollaries (C1, C2) to develop a comparator, whose bit size 'n' ranges between 2 and 32 as shown in Fig. 1. T1 computes A greater than B or B greater than A by processing 2-bit sub words of an n-bit number. T2 does a similar work except that it processes 3- bit sub words. T3 processes an n-bit number by considering two types of inputs, one of them is two bits i.e. n and n-1 and the other input is A greater than B or B greater than A computed for remaining n-2 bits. T4 also process n-bit numbers with inputs from the preceding stages. C1 computes A greater than B and B greater than A for an n-bit number by decomposing it into sub words of equal and unequal bit sizes. C2 serves as the equality checker for two n-bit numbers which considers the outputs of T1, T2, T3, T4 and C1 as its inputs. It also presents two different design styles, namely, Cascaded-based (CB) and Tree-based (TB) structures. Cascaded design approach process the input data bits in an interleaved or pipelined manner. It consumes increased MGs in the worst computational path or critical path, whereas in case of TB design, input data bits are processed through an efficient parallel architecture with fewer MGs. Existing design was in adequate to decide the topology, type and count of modules to meet minimum design requirements. The length of sub words processed by intermediate modules was also less. To overcome the limitations imposed in the existing work, a new method is proposed as Top-Down algorithm.

2. LITERATURE SURVEY

Designing forward leaps are expected to dispose of the size and foundation charge vacillations so as to stifle the edge voltage varieties. Single-electron draws near, speaking to a piece by a Single-electron ("bit state rationale") and the utilization of a solitary electron as a wellspring of irregular number ages, have been restricted to research center shows [1]. The issue of the restricted fan-

out, which is brought about by utilizing just a solitary electron in the really Single-electron designs, might be tackled by creative design plans, for example, the paired choice chart. Consequently, the lacks of CMOS have prompted noteworthy endeavors to discover proper other options and among the proposed arrangements; nano-scale advances, for example, Tunneling Phase Logic (TPL), Single Electron Tunneling (SET) and Quantum-dab QCA (QCA) have gotten extensive consideration [2]. Loathe looks into have proposed Quantum-spot potential executions for QCA cell. As such Quantum-spot cell has introduced in [3]. An adiabatic exchanging worldview is created for clock-controlled pipelined QCA designs. The double data is put away as electronic charge prompting less registering. Different examiners have been broadening the hypothetical examination of QCA clusters. Vankamamidi et al. [4] have proposed elective approaches of amassing QCA cell into helpful designs. They have created refined limited component models for door drained Quantum-dabs in semiconductors that can relate Dot inhabitance to specific predisposition conditions. They have introduced a basic timed atomic QCA cells. The particles show natural bistability because of dipole charge arrangement, which unequivocally couples to its neighboring atoms. The investigation is basic, characteristic just of the chance of utilizing sub-atomic QCA. Survey of the chance of executing QCA in sub-atomic scale or in nano-magnets has been done . A lot of atomic designs for QCA have been proposed, and one such 2-Dot QCA has been actualized. It is anticipated that a definitive utility of QCA will originate from joining presently existing innovations with cutting edge nanotechnology. Test utilization of QCA in Nano-scale Metal-speck characterized by burrow obstructions has been accounted for in [5]. Here the creators show a controlled polarization of QCA cells exchanging concurring with hypothetical predications. Timed QCA activity is exhibited on a case of a two cells move register. Examinations identified with exchanging pace and temperature reliance of QCA have been introduced in [6]. Customary Coulomb blocked and ace condition dynamic method has been mulled over for a semi-vast move register structure. The critical job of intensity gain as a component of temperature has been appeared. The conduct of such designs as capacity of clock speed and temperature is yet to be completely clarified [7]. It is discovered that design speed is constrained by RC-time steady, so Majority Voters could work up to 450-degree K, while QCA wire could work up to room temperatures.

3. EXISTING DESIGN

Quantum-speck QCA is a rising innovation which gives the different preferences, for example, quicker speed, littler size, and low force utilization and so on. The crucial design of QCA cells and can be utilized to plan the different kinds of designs (Combinational and consecutive). Therefore it is a central square of nano-electronic designs. This part expands the structure of QCA based combinational designs and gives a broad examination of proposed plans. This part talks about the different sorts of combinational designs which incorporate the ADD, SUB, MUXs, ENCs, Code converters and so forth. In this work all the designs have been structured utilizing the larger part doors.

4. PROPOSED ARCHITECTURE

There are two energetically unessential methods of two electrons in the QCA cells for an emptied cells, expected cells polarization P=+1 and cells polarization P=-1.while Cells polarization P=+1 insinuates equal 1 while cells polarization P=-1 implies relating 0.In extension, this idea is graphically depicted in figure - 1.It is also monster that there is an unpolarized state too. In an unpolarized state, potential purposes of control between contact are decreased which lessens the display commonly zero polarization and the two electron wave limits have been delocalized over the phones showed up in Figure 1

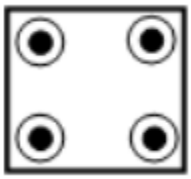

Fig 1.unpolarized cells

The numbering of spots meant by electrons in the phone goes clockwise start from the lattice on the upper suitable with quantum level I =1, base right cells I =2, base left cells I =3, and upper left cells i=4. The polarization level P in a cells is portrayed as Where Pi implies the electronic charge at spot current. The polarization appraises the charge plan for instance how much the electronic charge is appropriated among the four cell. The fundamental QCA reasonable design is the three-input greater part boolean operation (MG) that appears in Figure 5.2 from which dynamically complex designs can be created. The crucial MG doors are procured by setting four neighboring cell circumscribing to a quantum cells, which is in the inside. Three of the side cell are used as information sources, while the remaining one is the yield. The quantum cells will reliably expect the larger part polarization is the place there will be at any rate charge between the electrons in the three data cell and the quantum cells.

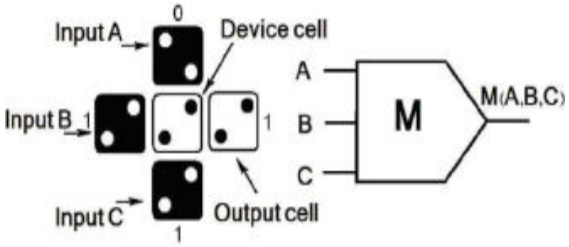

Fig 2.MG using QCA

Consider the columbic interface between cell 1 and 4,cell 2 and 4,cell 3 and 4 to see how the contraption cells achieves its most negligible criticalness state (and starting now and into the foreseeable future P=+1 in figure2).Typically, columbic relationship between electrons in cell 1and 4 would roll out 4 improvement its polarization considering electron shock. (Expecting

cells 1 is an information cells). Regardless, cell 2 and 3 in like way influence the polarization of cells 4 and have polarization P=+1. Thusly, considering the way that most of the phones impacting the contraption cells have polarization 1 P , it furthermore will besides expect this polarization in light of the fact that the powers of Columbic affiliation are more grounded for it than for 1.

Comparator is the basic unit in the digital circuit. As for 1-bit comparator, assuming the inputs are A and B, outputs are FA>B, FA

$$\begin{aligned} F_{A>B} &= A\overline{B} = M(A,\overline{B},0) \\ F_{A<B} &= \overline{A}B = M(\overline{A},B,0) \\ F_{A=B} &= AB + \overline{A}\overline{B} = \overline{M(M(A,\overline{B},0),M(\overline{A},B,0),1)} \end{aligned} \quad (1)$$

As for n-bit comparator, the outputs of one stage need to be the inputs of the next stage. For stage i, assuming the outputs are OA>B, OA

$$\begin{aligned} O^i_{A>B} &= O^{i+1}_{A>B} + O^{i+1}_{A=B}F^i_{A>B} \\ &= M_3(O^{i+1}_{A>B}, M_3(O^{i+1}_{A=B}, F^i_{A>B}, 0), 1) \\ O^i_{A<B} &= O^{i+1}_{A>B} + O^{i+1}_{A=B}F^i_{A<B} \\ &= M_3(O^{i+1}_{A>B}, M_3(O^{i+1}_{A=B}, F^i_{A<B}, 0), 1) \\ O^i_{A=B} &= O^{i+1}_{A=B}F^i_{A=B} = M_3(O^{i+1}_{A=B}, F^i_{A=B}, 0) \\ &Where\ i = (n-1, n-2 \ldots 0) \end{aligned}$$

In this paper, we use five-input majority gates to design comparator circuit to reduce the logic depth. For 1-bit comparator, the logic function of outputs can be shown as below:

$$\begin{aligned} F_{A>B} &= M_5(F'_{A>B}, F'_{A>B}, M(A,\overline{B},0), F'_{A=B}, 0) \\ F_{A<B} &= M_5(F'_{A<B}, F'_{A<B}, M(\overline{A},B,0), F'_{A=B}, 0) \\ F_{A=B} &= \overline{M(M(A,\overline{B},0),M(\overline{A},B,0),1)} \end{aligned} \quad (3)$$

A, B are the inputs of the current bitwhile F'A>B, F'AB,YAIt is easy to expand the 1-bit comparator to n-bit comparator. To improve the speed, the proposed comparator works from both high bit and low bit. Take the 4-bit comparator for example. Assuming A3 A2 A1 A0 and B3 B2 B1 B0 are the two inputs, YA>B, YA

$$\begin{aligned} Y_{A>B} &= M_5(K_1A, K_1A, K_1E, K_0A, 1) \\ Y_{A<B} &= M_5(K_1B, K_1B, K_1E, K_0B, 1) \\ Y_{A=B} &= M(K_1E, K_0E, 0) \end{aligned} \quad (4)$$

The logic functions of K1A, K1B, K1E, K0A, K0B, K0E are shown as follows:

$$K_1A = M_5(M(A_3,\overline{B_3},0),M(A_3,\overline{B_3},0),M(A_2,\overline{B_2},0),\overline{M_3(M_3(A_3,\overline{B_3},0),M_3(\overline{A_3},B_3,0),1),1})$$

$$K_1B = M_5(M(\overline{A_3},B_3,0),M(\overline{A_3},B_3,0),M(\overline{A_2},B_2,0),\overline{M(M(\overline{A_3},B_3,0),M(A_3,\overline{B_3},0),1),1})$$

$$K_1E = \overline{M(M(M(\overline{A_3},B_3,0),M(A_3,\overline{B_3},0),1),\overline{M(M(\overline{A_2},B_2,0),M(A_2,\overline{B_2},0),1),0})}$$

$$K_0A = M_5(M(A_1,\overline{B_1},0),M(A_1,\overline{B_1},0),M(A_0,\overline{B_0},0),\overline{M(M(A_1,\overline{B_1},0),M(\overline{A_1},B_1,0),1),1})$$

$$K_0B = M_5(M(\overline{A_1},B_1,0),M(\overline{A_1},B_1,0),M(\overline{A_0},B_0,0),\overline{M(M(\overline{A_1},B_1,0),M(A_1,\overline{B_1},0),1),1})$$

$$K_0E = \overline{M(M(M(\overline{A_1},B_1,0),M(A_1,\overline{B_1},0),1),\overline{M(M(\overline{A_0},B_0,0),M(A_0,\overline{B_0},0),1),0})}$$

The schematic diagram of the 4-bit comparator is shown as in Figure 4

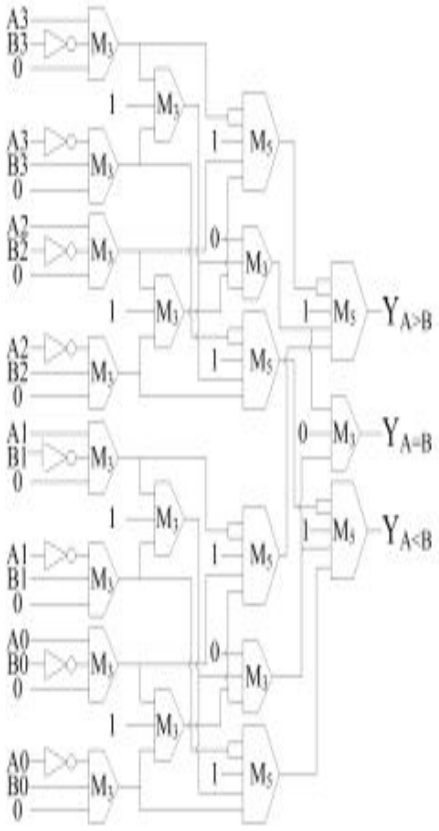

Fig. 3 Schematic of 4-bit comparator

Proposed 4-bit comparator is composed of 21 majority gates and 4 inverters. By using five-input majority gate,the length of the critical path decreased. There are four majority gates on the critical path.

5. SIMULATION OUTCOMES

5.1 Waveforms

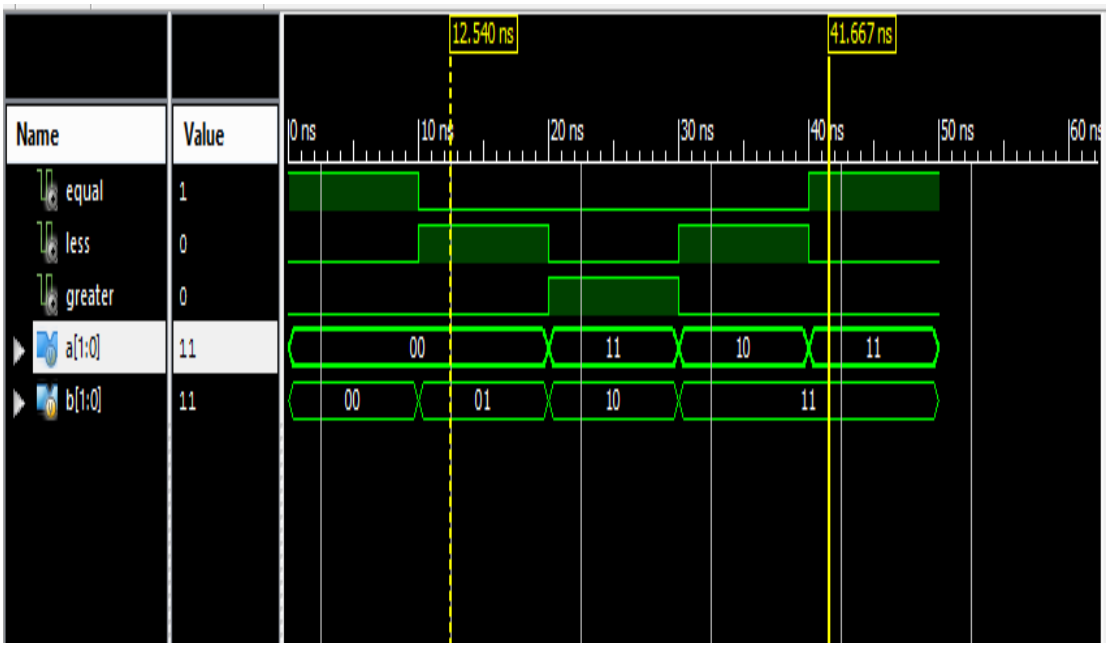

Fig. 4. Waveforms of 4-bit comparator

5.2 Design Summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	4982	204000	2%
Number of fully used LUT-FF pairs	0	4982	0%
Number of bonded IOBs	131	600	21%

Fig. 5. Design Summary of 4-bit comparator

The above outcome represents the synthesis design by using the Xilinx ISE tool. From the above table, it is observed that only 4982 LUTs are used out of available 204000. It indicates very less area (2%) was used for the proposed design

5.3 Time Summary

```
LUT2:I0->O            1   0.043   0.000  div1/Madd_GND_49_o_GND_49_o_a
MUXCY:S->O            1   0.230   0.000  div1/Madd_GND_49_o_GND_49_o_a
XORCY:CI->O           2   0.251   0.347  div1/Madd_GND_49_o_GND_49_o_a
LUT4:I2->O            1   0.043   0.000  div1/Msub_n0258_Madd_lut<30>
MUXCY:S->O            0   0.230   0.000  div1/Msub_n0258_Madd_cy<30> (
XORCY:CI->O           1   0.251   0.289  div1/Msub_n0258_Madd_xor<31>
LUT5:I4->O            1   0.043   0.279  Mmux_out110 (out_0_OBUF)
OBUF:I->O                 0.000          out_0_OBUF (out<0>)
---------------------------------------
Total                    54.238ns (31.895ns logic, 22.343ns route)
                                  (58.8% logic, 41.2% route)
```

Fig.6. Time Summary of 4-bit comparator

The above outcome represents the time consumed such as path delays by using the Xilinx ISE tool. The consumed path delay is 54.238ns.

5.4 Power Summary

Device	
Family	Virtex7
Part	xc7vx330t
Package	ffg1157
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	3709	204000	2
Signals	0.000	4570	--	--
IOs	0.000	131	600	22
Leakage	0.143			
Total	0.143			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.4	84.8	25.2

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.086	0.000	0.086
Vccaux	1.800	0.030	0.000	0.030
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.143	0.000	0.143

Fig.6. Power Summary of 4-bit comparator

The above outcome represents the power consumed by using the Xilinx ISE tool. The consumed power is 0.143uw.

5.5comparasion Table

parameter	EXISTING APPROACH[1]	PROPOSED APPROACH
Time delay	59.110 ns	54.238 ns
Power utilized	1.293uw	0.143 uw
Look up tables	5277	4982

6. CONCLUSION

In this project, another QCA based with N-bit Comparators plans has created to play out the number-crunching and coherent tasks. The reenactment outcome affirms the proposed tasks have created with less cell, zone and inertness. Moreover, to diminish the inconvenience of the expansion related activities, capable Comparators have been proposed. The utilization and reproduction outcomes shows that the proposed technique furnishing a lot of the better execution regarding the region, force and deferral.

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