# Performance Assessment of a Single Phase 7 Level Z-Source Boost Inverter in Real Time

Pinjari Rajavali M.Tech Student Dept. of Electrical and Electronics Engineering Anantha Lakshmi Institute of Technology and Sciences Ananthapuramu B. Mallikarjuna Assistant Professor Dept. of Electrical and Electronics Engineering Anantha Lakshmi Institute of Technology and Sciences Ananthapuramu

#### Abstract

Multilevel inverters are a well-known and widely used topology for converting DC to AC power. This study presents a seven-level Z source diode clamp multilevel inverter's realtime performance progression. The primary hardware platforms for real-time simulations are computer clusters, and field programmable gate array (FPGA) integrated real-time simulators. The parallel simulation of an electrical circuit on groups of personal computers operating at a sampling rate of 10 ps is made possible by the real-time (RT) lab software. High-power applications with minimal total harmonic distortion use DC-AC converters that integrate multilevel inverters with z-source energy conversion. Two passive components are between the DC power source and the multilevel inverter circuit, such as two inductors and two capacitors. As opposed to the traditional multilevel inverter, it offers a particular function that boosts the inverter output voltage and lowers the harmonic content in the output voltage. The suggested system's real-time findings are validated using a predetermined time step of 10 s and a frequency of 10 KHz.

**Keywords:** Field programmable gate array, multilayer inverter, software in the loop, realtime digital simulators, etc.

# I. INTRODUCTION

Real-time digital simulators with embedded FPGAs (RTDS) are newly developed instruments employed in various settings, including industrial applications, automation, the power sector, electrical drives, and engineering education. Because it operates for highperformance industrial applications in real-time precision, RTDS is a challenging and comprehensive research field [13]. While the simulation was running, it was possible to modify the system's reference settings and assess how it performed dynamically. It is not possible in offline simulation software packages like PSIM, MATLAB/Simulink, PSCAD, and PSPICE, among others. Offline simulation solutions have limitations such as a changeable time-step solver, time commitment, inability to interface with real hardware, and execution on a single CPU. RT-LAB functions in real-time contexts and is wholly integrated with MATLAB/Simulink. Before actual field implementation, a bridge between the theoretical concept and hardware prototype system design is built using real-time simulation findings. Using intervening simulators with real-time communication links, RTDS can distribute the load across multiple CPUs. Real-time simulations use a variety of control mechanisms, including hardware and software, in the loop. With a virtual simulation environment to create the hardware prototyping system, Software-in-the-Loop (SIL) simulation symbolises the integration of source code into a mathematical model simulation. It may directly and interactively test and edit its source code using a PC and is an excellent addition to traditional HIL simulation. Additionally, it aids in accelerating time-to-market and ensuring that software development is more significant. By identifying and managing faults more quickly earlier in the process and spending less time debugging, this technique also cuts down on the overall project hours. Engineers may evaluate a broader range of properties with HIL simulation than they can with a straightforward support setup. This makes it possible to

test the effectiveness of the equipment using a more comprehensive range of metrics, traits, and flaws. The ability to try a variety of frameworks, including power converters, generators, engines, and PV stacks, is provided to architects. The method also allows testing inverter worms without using complicated technologies. Simply put, PHIL testing enhances activity well-being and produces products and frameworks that are more secure. Before developing hardware and deploying it in the field, design and testing were crucially important. Such models are shown mathematically on a computer during the simulation phase. Numerous publications on the performance of bidirectional quasi-inverter drives [4], modified z-source inverter drives [5], modelling and dependability of AC-AC converters [6], and quasi-z-source inverter drives [7] have been published in the literature.

The term "multilevel inverter" (MI) refers to a popular DC-AC converter topology that creates a sinusoidal voltage from many voltage levels. In particular, medium- and highvoltage applications, including AC motor drives, STATCOM, grid-connected systems, uninterruptible power supply, and grid-to-renewable energy source connections, require MI. MI provides several advantages, including sinusoidal output waveforms, lower switching losses, higher output voltage capabilities with fewer harmonics, improved efficiency, reduced dv/dt stresses, and reduced common-mode voltage effects. The appealing qualities of both the multilevel inverter and z-source inverter have been introduced with the integration of a multilevel z-source power converter. Single-stage boost converter, low overall harmonic distortion, high power conversion, and lower switching voltage stresses across semiconductor devices are the benefits of z-source multilevel inverters over standard multilevel inverters. Multilevel inverters come in various designs, including H-bridge, flying capacitor, and neutral diode clamped [8-9]. To regulate multilevel inverters, the research [10] discussed model predictive control (MPC) approaches that combine finite at MPC with specific harmonic elimination (SHE). The formulation of ML-ZSI employing waveform integration and approximate methods has been described in the paper [11]. Techniques for compensating for sag and swell circumstances in the power system are presented using the z-source multilayer inverter with a reduction switch [12].

When compared to a conventional multilevel inverter, the z-source diode clamp inverter has the following advantages:

- The output voltage of the inverter has the fewest harmonics possible
- Lessening of voltage strains across semiconductor switching devices
- Operating as a second-order filter is the impedance network
- The minimal inductance needed for a similar switching frequency decreased total harmonic distortion in the output and also improved inverter efficiency. Clamping diodes must be used more significantly to compensate for the issues. Fig. 1 shows the multilayer inverter's block diagram.

Using third harmonics injected boost control techniques, the input diodes require the fewest components.

The traditional multilayer inverter does not produce buck mode or shoot-through states because it generates less than the input voltage. The integrated diode clamp for the z-source To increase the inverter output voltage while excluding any indemnification from the circuit, a Z-source inverter is used in the shoot-through (ST) condition. One stage boost voltage capability, which means that AC power output is more significant than DC input power, component reduction, and shoot-through immunity are some appealing characteristics of the suggested system [13–16].

#### **II PROPOSED SYSTEM**

The traditional multilevel inverter acts like a buck converter, meaning that the AC output is lower than the source voltage. Renewable energy sources are used for high power in

typical applications using a DC-DC converter before the voltage source inverter. The input source and the multilevel inverter bridge circuit are inductors and capacitors elements of an impedance network. Fig. 1 shows the z-source multilevel inverter's block diagram. The traditional neutral clamp diode inverter does not have shoot-through states since it shorts out the capacitors on the DC side. It functions in three different modes, including the well-known shoot-through state, active state, and zero states. No electricity is transferred across the load during the zero condition. Employ the shoot-through duty ratio to increase the inverter's output voltage and reduce distortion in the AC output voltage.

The DC power input impressed across the load when the system was operational. Its distinguishing feature is the Z source converter's ability to produce a wide range of AC output voltage while controlling the shoot-through duty ratio and minimising total harmonic distortion in the AC voltage. The gate pulses for the IGBT switches are provided via control signalling that uses the third harmonics injected constant boost control approach. It has more basic voltage and less low-order harmonic content than conventional PWM modulation control approaches. The seven-level diode clamp z-source multilevel inverter with resistive load's circuit structure is depicted in Fig. 2. The neutral clamped inverter is another name for the diode clamped inverter. Utilising the control signal's shoot-through state and modulation index, the z-source multilevel inverter's output voltage can be used. The suggested structure used various levels of DC voltages produced by DC capacitors to achieve the sinusoidal output voltage. If n is a defined level, then (n-1) capacitors are required on the DC bus, (n-1) semiconductor IGBT switches are necessary for each phase, and (n-1) diodes are required for each stage (n-1). Clamping diodes and one capacitor can correct the voltage stress. By raising the inverter's levels, overall harmonic distortion in the output is reduced, and the inverter's efficiency is also increased. Clamping diodes must be used more significantly to compensate for the issues.



Fig. 1 Block diagram of multilevel inverter

The inverter output voltage is expressed as MD Vir / 2 = M [(1/(1 - 2D))] (Vir / 2)

Voutput = MB Vin/2 = M [(1/(1-2D)] (Vin/2) B defines the boost factor M defines the control signal's mode

B defines the boost factor, M defines the control signal's modulation index, and D represents the shoot-through cycle duty.

# **III. RESULTS AND DISCUSSIONS**

FPGA-integrated real-time simulators perform the seven-level z-source inverter systems' real-time performance with MATLAB/Simulink interfaces. The system's simulation settings are as follows: input voltage = 100 V DC, load R = 50 Q, switching frequency = 10 KHz, modulation index = 1, impedance networks parameters: inductors L1 = L2 = 40 mH, capacitors C1 = C2 = 6000 pF. The proposed control signal PWM pulses in the simulator are executed at predetermined intervals of 10 s, with a defined fixed switching frequency of 10 KHz. The concerned IGBTs of the inverter receive the gate signal from the pulse generator. By controlling the shoot-through ratio, the inverter voltage level is increased. The performance of the z-source multilevel inverter with various shoot-through duty ratios is shown in Table 1. Fig. 3 displays the voltage waveforms of seven-level z-source inverters in real-time simulation. The system's boost factor is determined to exceed that of conventional multilayer diode clamp inverter techniques. A shoot-through (ST) state is utilised in the diode clamp z-source inverter to increase the inverter output. The input power is affected across the load during a non-shoot-through condition, and no power is transferred to the bag during a zero state. Figures 4 and 5 show the hardware-in-loop (HIL) simulation waveforms of the

multilayer z-source inverter output voltage and impedance network capacitor voltage, respectively. In comparison to a standard multilevel inverter, a Z-source multilevel inverter provides a 20% greater boost capability for the inverter output voltage level. According to Fig. 6, THD in the Z source multilevel inverter output voltage is 22.53 per cent.



Fig. 2 Seven-level diode clamp z-source multilevel inverter



Fig. 3 Real-time simulation waveform of seven-level z-source inverter output voltage



Fig. 4 Hardware in loop simulation waveforms of seven-level inverter output voltage

TABLE I The Execution of Inverter Output Voltage at Different Shoot-Through Duty Cycle

Shoot-through duty ratio	Boost factor (B)	Output voltage (rms) Volts
0.05	1.11	119.88
0.10	1.25	135.00
0.15	1.43	154.44
0.20	1.67	197.85
0.25	2.00	216.00
0.30	2.50	270.00
0.35	3.33	359.64



Fig. 5 Hardware in loop simulation waveforms of capacitor voltage

# **IV. CONCLUSIONS**

This paper describes the multilevel z-source inverter's real-time performance implementation on an FPGA. The suggested model is run using fixed time frame step algorithms in an integrated FPGA simulator, which reduces computing costs while maintaining result accuracy. It offers the best output results compared to an offline simulation tool like the MATLAB/Simulink environment. The advantages of a multilevel z-source inverter include using an impedance network, which lowers THD in the output voltage and has more boost capacity than a traditional multilevel inverter. The impedance network also functions as a second-order filter to increase efficiency and remove lower order harmonic content from the output voltages. Numerous benefits of the suggested approach include the output voltage level. For motor drives, STATCOM, and integrated grid systems for renewable energy, z-source multilevel inverters can be employed for high output voltage with lower order harmonics in the output. Using FPGA-based simulators, the simulation results were used to validate the performance of the seven-level multilevel inverter.

# REFERENCES

[1] M. Ashourloo and et al., "Enhanced model and real time simulation architecture for modular mutilevel converter," IEEE Trans. on Power delivery, vol. 33, pp. 466-476, 2017.

[2] J. Enayati and Z. Moravej, "Real time harmonics estimation in power systems using a novel hybrid algorithm," IET Gen. Trans and Distribution, vol. 11, no. 14, 2017.

[3] S. Mojlish and et al., "Review of hardware platforms for real time simulation of electric machines," IEEE Trans. on Transpotation Electrifications, vol. 3, no. 1, pp. 130-146, 2017.

[4] H. Prasad and T. Maity, "Real time simulation for performance evaluation of bidirectional quasi z-source inverter based medium voltage drives," COMPEL, The Int. Journal for Com. and Math. in Elec and Elect, vol.35, 2016.

[5] H. Prasad and T. Maity, "Real time performance analysis of modified z-source inverter fed induction motor drives using Xilinx system generator," European Power Electronics, vol 26, pp. 142-152, 2016.

[6] H. Prasad and T. Maity, "Modeling and reliability analysis of three phase z-source AC-AC converter," Arch. of Elec. Engg, vol. 66, no. 4, pp. 731-743, 2017.

[7] T. Maity and H. Prasad, "Real time performance evaluation of quasi z-source inverter for induction motor drives," 26th IEEE Inter. Sym. on Ind. Electronics, pp. 844-849, 2017.

[8] J. Lai and F. Z. Peng, "Multilevel converters A new breed of power converters," IEEE Trans. on Ind. App. vol. 32, 1996.

[9] J. Rodriguez and et. al. "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. on Ind. Elec. Vol. 49, no. 4, pp. 724-738, 2002.

[10] R. P. Aguilera and et al., "Selective harmonic elimination model predictive control for multilevel power converters," IEEE Trans. on Power Elect. vol. 32, no. 3, pp. 2416-2426, 2017. [11] M. S. Pilehvar and et. al., "Formulation of phase voltage and caculation of its total harmonic distortion in z-souce inverter," IET Power Elec. Vol. 8, no. 8, pp. 1509-1518, 2015.
[12] M. R. Banaei and et. al. "Z-source based multilevel inverter with reduction of switches," IET Power Elec. vol. 5, no. 3, 2012.

[13] A. P. Mattavelli at. Al., "Three phase three level flying capacitors split source inverters anlysis and modulation," IEEE Trans. on Ind. Elec. vol. 64, 2017.

[14] M. Sahoo and S. Keerthipati, "A three level LC switching baased voltage boost NPC inverter," IEEE Trans. on Indus. Elec., vol. 64, pp. 2876-2883, 2017.

[15] M. Nguyen and T. Tran, "Quazi cascaded H-bridge five level boost invereter," IEEE Trans. on Indus. Elec. vol. 64, pp. 8525-8533, 2017.

[16] A. Ho and T. Chun, "Single phase modified quasi z-source cascaded hybrid five level inverter," IEEE Trans. on Ind. Elec., vol. 65, 2017.