IMPLEMENTATION OF 3-PARALLEL POLYPHASE ODD LENGTH FIR FILTER USING BRENT KUNG ADDER AND BOOTH MULTIPLIER FOR VLSI APPLICATIONS

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ABSTRACT: In digital signal processing, an FIR is a filter whose impulse response is of finite period, as a result of it settles to zero in finite time. This is often in distinction to IIR filters, which can have internal feedback and will still respond indefinitely .This paper presents the utilization of a FFA based 3-parallel polyphase FIR filter with optimized adders and multipliers instead of traditional adders and multipliers. Specifically, a FFA based 3-parallel polyphase odd length FIR filter is proposed using two different multipliers - Vedic multiplier and Booth multiplier - and three different adders - Ripple carry adder, Carry lookahead adder, and modified Brent Kung adder .It is used to reduce the complexity of the circuit when compared to using Brent kung adder . The modifications occur in Efficient 3-parallel polyphase odd length FIR filter using Brent Kung adder and Booth multiplier for VLSI applications is instead of Brent kung adder we use modified Brent kung adder for reducing complexity and more efficient of circuit. We implement using Xilinx and simulate using modelsim software.

1.INTRODUCTION:

In the domain of Very Large Scale Integration (VLSI) applications, the demand for high-performance digital signal processing (DSP) circuits has become increasingly prevalent. Finite Impulse Response (FIR) filters, known for their stability, linear phase response, and ease of implementation, constitute a fundamental component in various digital signal processing systems. However, as the requirements for higher throughput and lower power consumption escalate, there is an imperative need for innovative techniques to design efficient and optimized FIR filters.

This project focuses on the development of an efficient 3-parallel polyphase odd-length FIR filter tailored for VLSI applications, utilizing the prowess of the Brent Kung adder and Booth multiplier. The 3-parallel polyphone structure has been selected due to its ability to enhance processing speed and mitigate hardware complexity. By incorporating the Brent Kung adder, renowned for its low propagation delay and high-speed addition capabilities, alongside the Booth multiplier, known for its efficiency in reducing partial product terms, the proposed design aims to achieve enhanced computational performance and reduced power consumption.

The utilization of these advanced hardware architectures within the context of the polyphase FIR filter design is expected to yield notable improvements in terms of speed, area utilization, and power efficiency, making it an ideal solution for demanding

VLSI applications. This project seeks to demonstrate the potential of this integrated approach and explore its applicability in various high-speed signal processing applications such as communications, multimedia processing, and digital signal processing systems, thereby addressing the pressing need for efficient and high-performance FIR filters in contemporary VLSI designs.

Through comprehensive analysis, simulation, and synthesis, the proposed design aims to provide valuable insights into the practical implementation of advanced architectures, offering a robust foundation for future research and development in the realm of VLSI-based digital signal processing

In the world of Very Large Scale Integration (VLSI) applications, the development of efficient digital filters plays a crucial role in signal processing tasks. One important type of filter is the Finite Impulse Response (FIR) filter, which is widely used for tasks like noise reduction, signal equalization, and data compression. This discussion focuses on enhancing the efficiency of a specific type of FIR filter - the 3-parallel polyphase filter with an odd length. To achieve this, we will employ advanced arithmetic components like the Brent Kung adder and the Booth multiplier. These components are designed to optimize the filter's computational speed, making it well-suited for real-time processing applications in VLSI circuits. This exploration aims to provide a clear understanding of how these advanced techniques can be integrated to improve the performance of digital filters in VLSI systems

2. LITERATURE SURVEY:

VLSI Digital Signal Processing System : Design and Implementation by K.K.Parhi. Digital audio, speech recognition, cable modems, radar, high-definition television- these are but a few of the modern computer and communications applications relying on digital signal processing (DSP) and the attendant application-specific integrated circuits (ASICs). As information-age industries constantly reinvent ASIC chips for lower power consumption and higher efficiency, there is a growing need for designers who are current and fluent in VLSI design methodologies for DSP.

Design and implementation of area efficient 2-parallel filters on FPGA using image system by L. K. Phimu and M. Kumar. Parallel FIR filter is mostly used among various types of filter in Digital Signal Processing (DSP). This paper shows the design of area-efficient 2-parallel FIR filter usingVHDL and its implementation on FPGA using image system. This paper gives the details basic blocks of area-efficient 2-parallel FIR digital filter. In this paper proposed 2-parallel digital FIR filter and area-efficient 2-parallel FIR filter are explained. Its simulation using Xilinx 14.2 are also discussed. It also presents the FPGA implementation of primary 2-parallel filter and area-efficient 2-parallel on Xilinx 14.2 Spartan 3E Starter Board XC3S500E chips and its results. Since adders are light weight in silicon area when compare with the multipliers, therefore multipliers are replaced by the adder to reduce areaand delay of the parallel FIR filter. Xilinx ISE is used for simulating the design of the filter.

Short-length FIR filters and their use in fast nonrecursive filtering by Z.-J. Mou, and P. Duhamel

The basic tools required for an efficient use of the recently proposed fast finite impulse response (FIR) algorithms are provided. These algorithms not only reduce arithmetic complexity but also partially maintain the multiply-accumulate structure, thus resulting in efficient implementations. A set of basic algorithms is derived, together with some rules for combining them. Their efficiency is compared with that of classical schemes in the case of three different criteria, corresponding to various types of implementation. It is shown that this class of algorithms (which includes classical ones as special cases) makes it possible to find the best tradeoff corresponding to any criterion

Hardware-efficient VLSI implementation for 3-parallel linear-phase FIR digital filter of odd length by Y.C. Tsao, and K. Choi. Based on fast FIR algorithms (FFA), this paper proposes new 3-parallel finite-impulse response (FIR) filter structures, which are beneficial to symmetric convolutions of odd length in terms of the hardware cost. The proposed 3-parallel FIR structures exploit the inherent nature of the symmetric coefficients of odd length, according to the length of filter, (N mod 3), reducing half the number of multipliers in subfilter section at the expense of additional adders in preprocessing and postprocessing blocks. The overhead from the additional adders in preprocessing and postprocessing blocks stay fixed, not increasing along with the length of the FIR filter, whereas the number of reduced multipliers increases along with the length of the FIR filter. For example, for a 81-tap filter, the proposed A structure saves 26 multipliers at the expense of 5 adders, whereas for a 591-tap filter, the proposed structure saves 196 multipliers at the expense of 5 adders still. Overall, the proposed 3-parallel FIR structures can lead to significant hardware savings for symmetric coefficients of odd length from the existing FFA parallel FIR filter, especially when the length of the filter is large.

Hardware-efficient parallel FIR filter structure based on modified Cook-Toom algorithm by Q. Tian, Y. Wang, G. Liu, X. Liu, J. Diao, and Hui Xu. The Cook-Toom algorithm is widely used in short-length linear convolution, which is the building block of large points convolution algorithms. This paper proposes improved parallel finite impulse response (FIR) filter structures for linear-phase FIR filter, which is based on the Cook-Toom algorithm. In the proposed structures, Cook-Toom algorithm is used to reduce the number of sub-filters, and the symmetric properties of the linear-phase FIR filter's coefficients is used to further reduce the number of multipliers in sub-filters. Compared with the reported FFA and ISCA parallel FIR filter structures, the proposed method can substantially reduce the computational complexity. Specifically, for a 8-parallel 144-tap filter, the proposed design saves 18 multipliers (5%), 45 adders (7.9%) compared with the structure based on Winograd convolution algorithm [7].

3.EXISTING SYSTEM:

In this system we use different multipliers like array multiplier, vedic multiplier, Booth multiplier in this array multiplier has two steps partial product generation and final summation but using of this multiplier we can face a problem that carry incrimination

it reduces the efficiency of the circuit so we use Booth multiplier and Brent Kung adder. Implementation of two different multipliers and three adders. This is followed by separate comparisons among the adders and the multipliers. From these comparisons, it can be concluded that the 3-parallel polyphone odd length FFA based FIR filter design using Brent Kung adder and Booth multiplier gives best result among multipliers and adders respectively. from the existed system the using of Brent Kung adder face more complexity it is the disadvantage.

4. PROPOSED SYSTEM:

FIR filter is the most widely used DSP technique. The N-tap FIR filter is normally described by the following equation.

$$y(n) = \sum_{k=0}^{N-1} h(i)x(n-i),$$

(1)

Where N is the number of coefficients (or taps) of the filter, h[n] represents filter coefficients, x[n], y[n] are the input and output sequences respectively. The N-tap FIR filter is characterized by N coefficients and in general, requires N multipliers and (N-1) two-input adders for implementation. Structures in which the multiplier coefficients are the same as the coefficients of the transfer function are called direct-form structures. A direct-form realization of an FIR filter can be readily developed from Eq.(1) as indicated in Figure 1 for N=4.

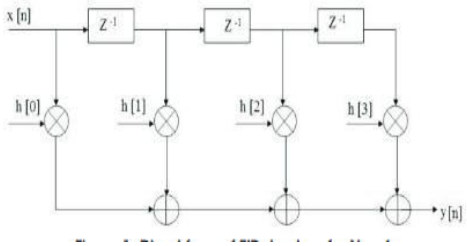

Fig 1. Direct form of FIR structure for N = 4

In proposed system we can overcome the disadvantage of existed system which is using of Brent Kung adder there is complexity in circuit to reduce the complexity we use modified Brent Kung adder. The Modified Brent-Kung adder is a parallel prefix adder that improves on the Brent-Kung adder by reducing the critical path delay. It employs a modified structure for the carry-look ahead unit, resulting in enhanced performance compared to the original design. If you have specific questions or aspects you'd like to discuss about the Modified Brent-Kung adder

Booth Multiplier

Booth multiplier can multiply two signed and unsigned binary values using 20s complements with great accuracy. Additional advantages include low power consumption and faster computation. In this multiplier a operand is chosen as a multiplier which acts as loop count of algorithm, another operand acts as multiplicand on which Airthmetic shift is performed. As the loop count becomes zero sum is obtained as shown in Fig.2.

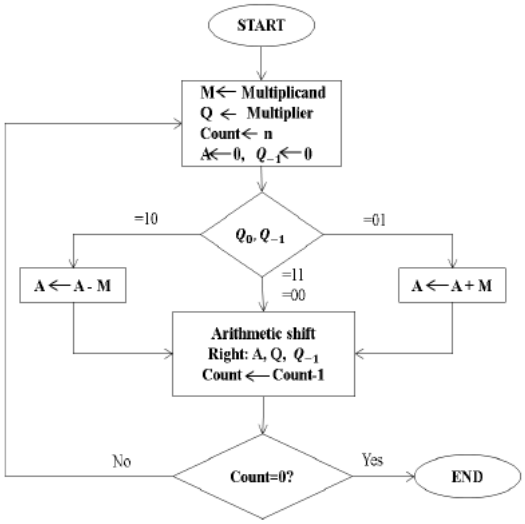

Fig. 2. Booth Multiplier

Brent Kung Adder

Parallel prefix adder architectures contain tree like structures which compute the required carry input (carry)I for every bit of addition. The tree structures are developed by using different operators, which receive, generate and propagate signals of previous level and compute, generate and propagate signals for next level. The realization of these operators, for enhancement of speed characteristic is also developed. The hybrid architecture of parallel prefix tree is presented for high speed area efficient characteristics.

It is a post prefix adder that is a revised version of the Carry look ahead adder. Brent Kung adder shown in Fig.2 produces rapid results, is easy to construct, uses a small number of nodes and saves power. It is regarded as one of the most flexible adder. The addition process involves following three stages:

1.Pre-processing stage.
2.Carry generation network.
3.Post-processing stage.

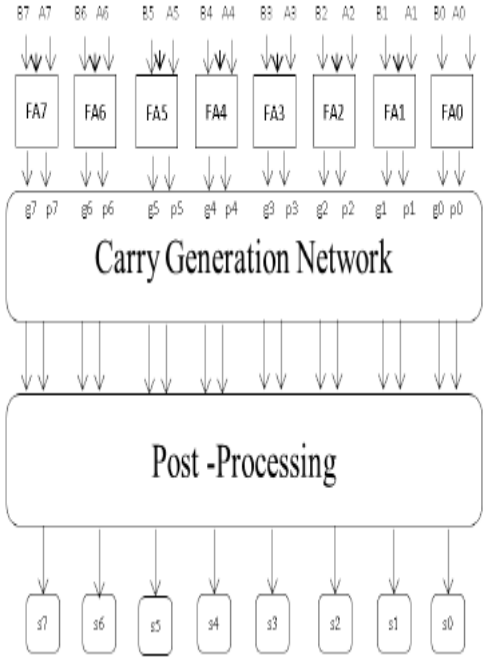

Fig. 3. Brent-Kung Adder

5.SIMULATION RESULTS

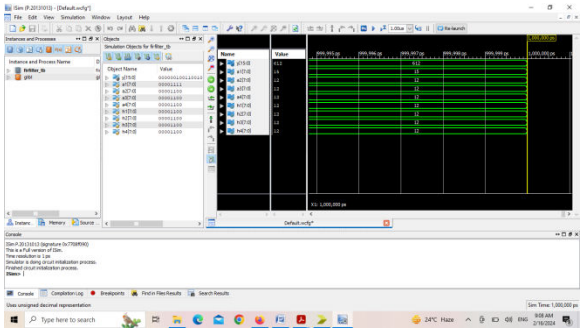

Fig 4 Simulation results

6.CONCLUSION

The parallel FIR filter plays very important role in Digital Signal Processing. With the advancement in the technology, less chip area and low power consumption is the primary focus of FIR filters design using VLSI technology. The parallel FIR filter contains three units: adder, multiplier, and delay. The multiplier is the slowest among all the units, adder also contributes in slowing the process. To get efficient multiplier and adder, the 3-parallel polyphase FFA based odd length FIR filter has been designed using two different

multipliers and three different adders. In this research paper the presented idea was able to achieve adequate results. It is evident from the results that chip area and power dissipation of 3-Parallel polyphase odd length FIR filter designed using Brent Kung adder and Booth multiplier is significantly reduced, hence making the system faster.

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