IMPLEMENTATION OF DLATCH AND FLIP FLOP USING MEMRISTOR LOGIC

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ABSTRACT: Sequential devices are the fundamental building blocks for almost all digital electronic systems with memory. Due to the importance of instant data recovery after unexpected data loss such as unplanned power down, sequential devices need to have the nonvolatile property, which motivates the recent research and practice in integrating the nonvolatile memristor into CMOS devices. In this project, we study how to apply this approach to improve the quality of nonvolatile D latch. Unlike the structure of conventional design, the proposed D latch consists of only one memristor, several transmission gates, and CMOS inverters. Our design overcomes the negative effect due to the threshold loss of the transistors. As simulation shows, compared with the current designs, our proposed memristor-based D latch can support the memristor to switch between different resistance states 2.3X-3.6X faster, and thus achieving a clock of higher frequency. In addition, our design allows the threshold value of the memristor to be selected from a much wider range. As an application, we use the proposed memristor-based D latch to implement a nonvolatile masterslave D flip-flop, which has smaller delay than all the state-of the- art designs and smaller area than all but one of them. Our designs improve the quality of memristor-based D latch and D flip-flop in terms of latency, area, and flexibility of threshold voltage selection, making them a promising option for data backup in real life systems.

1. INTRODUCTION

In the era of big data, data protection is vital and challenging because no one can predict where and when the next downtime will occur. Data backup technology is one of the best solutions in practice to minimize data loss and other negative impacts. Therefore, the efficiency in data backup and restoring will determine whether the system can maintain a continuous and stable operation.

During the backup process, data stored in the volatile memory will be transferred to the nonvolatile memory and restored after downtime ends. The latency for the data transportation mainly depends on the type of memory and the structure of the system. How to minimize such latency becomes crucial for the efficiency of data backup. Flip-flops and latches are the fundamental building blocks of digital electronic systems. Traditional flip-flops are volatile memory and will lose the data they store in case of a power interrupt. Many techniques have been proposed to implement the maintenance of the intermediate state of flip-flops. One interesting approach that recently gains a lot of attention is to exploit various emerging memory technologies, including ferroelectric RAM, phase change RAM, spin-transfer torque magnetic RAM, and ferroelectric transistor, to maintain the volatile content in flip-flops for data backup and restoration operations. These schemes integrate nonvolatile memory components and the corresponding control circuit into the conventional CMOS flip-flop to reduce both latency and power consumption, and hence improving the quality of flipflop design and data backup.

To overcome this issue, many approaches have been taken, such as caching – storage of

frequently used data in a special area (usually random access memories, RAM), so that it is more readily accessible than the main memory –, prefetching moving some data into cache before it is requested to speed access in the event of a request –, multithreading – managing multiple requests simultaneously in separate threads. These conditions gave birth to a memory hierarchy. This hierarchy is based on the price per bit, the size of the memory and the transfer rate. In the first tier are the static random-access memories (SRAMs), which are integrated into the processor to enable fast data access. They have the best transfer speed with high cost per bit, both in device area (6 transistors, 6T) and financial. In the next tier are the dynamic random-access memories (DRAMs), used for main memory. These memories need constant refreshes to maintain the data, so it generates more heat than the SRAMs but are much smaller (1T1C, 1 capacitor) and cheaper. Disk drives and NAND-based solid-state storage drives (SSDs) are used for storage. In the last tier are the hard disk drives (HDD). Both these categories are very slow, but cheap, so usually they have the biggest storage capacity in terms of bytes.

2. LITERATURE SURVEY

A. A nonvolatile latch circuit based on memristors." 235203 in Nanotechnology 21 & 23 (2010). Warren, Gilberto Medeiros-Ribeiro, Qiangfei Xia, Greg Snider, Robinett, Matthew D.

Volatile memory devices store data in various connection states and may therefore be employed in volatile computing systems. Excitation history affects the dynamic conduction state of these devices. The non-volatile memory is a nanoscale memory device in this article's construction of a synchronous flip-flop. State storage and retrieval are successful via controlled circuit testing. These results suggest that dispersed power sources and a combination of memristors and digital logic devices might enable nonvolatile computing on compact platforms. The traditional memory hierarchy holds that non-volatile memory can only be accessed as a huge, slow monolithic at the bottom of the hierarchy, however, the ability to tightly integrate memristors with CMOS (complementary metal-oxide-semiconductor) circuits undermines this assumption. Non-volatile memory cells built on memristors are fast, accurate, and compact enough to be integrated into standard CMOS circuits. As a result, the traditional memory hierarchy is put to the test, and new design possibilities are made available.

B. Zero-Sleep-Leakage Flip-Flop Circuit with Conditional-Storing Memristor Retention Latch," in IEEE Transactions on Nanotechnology C. -M. Jung, K. -H. Jo, E. -S. Lee, H. M. Vo and K. -S. Min

To effectively eliminate sleep leakage, two innovative non-sleep leakages (F-F) flip-flop (F-F) circuits have been developed. Data is sent from the F-F to the memristor retention latch during sleep, preventing the F-F from being completely disconnected from the external power source and power leakage during sleep. Compared to F-F, the conditional storage circuit of F-F (Type-2) can use less switching power to store data (Type 1). Additionally, compared to F-F, F-F (type 2) has a shorter crossover time (type 1).

C. Memristor-based nonvolatile synchronous flip-flop circuits J. Zheng, Z. Zeng, and Y. Zhu

Flip-flops are crucial parts of all varieties of sequential logic circuits and sophisticated digital electronics systems and may be utilized to store binary data due to their two stable logic states of 0 and 1. Digital circuits often make use of SR and D flip-flops as examples of basic base-flips. This work introduces non-volatile synchronous SR flip-

flop and D-flip-flop synchronous logic circuits that use non-volatile nano-memristors with various conduction states for data storing. components of memory. Memristors are the best choice for flip-flop circuits that need trigger functions since they can substitute resistors. In contrast to traditional flip-flops, the memristor-based SR flip-flop and D flip-flop have non-volatile properties that make them appropriate for applications with erratic power sources. Advanced circuits serve as empirical benchmarks for creating digital circuit topologies because tight memristor integration with CMOS circuits is feasible.

D. Determining optimal switching speed for memristors in the neuro morph systems stem. Electronics Yakopcic, C. &Taha, T.M. (2015).

Memristors with very fast switching times are becoming increasingly popular with the development of non-volatile memory based on resistive switching. On the other hand, according to the research mentioned above, memristors with modest switching times (around 10 seconds) are more suitable for use in nervous systems. This is achieved by simulating different types of memories with different switching times. Using each of these model components, a neural circuit based on memristors is simulated. To slowly adjust the memristor resistance in devices with high switching speeds, unreasonably low voltage pulses are required.

3. EXISTING SYSTEM

Different from the conventional SR flip-flop and D flip-flop circuits which consist of several logic gates, the proposed nonvolatile synchronous SR flip-flop and D flip-flop, discussed in this work, is based on the combination of CMOS and threshold-type voltage-controlled bipolar memristors. This section explains the topologies and operating principles of the flip-flops.

The schematic of the memristor is shown in Fig, bottom terminal is denoted by the black thick line. The memristance will decrease when the forward bias voltage is applied to acrthe oss memristor, and it will increase when the memristor is reversely-biased. In Fig, we show the qualitative current-voltage characteristic of the threshold-type switching memristor.

When the applied voltage is larger than the positive threshold VSET, the memristance switches to RON. Then, when the applied voltage is smaller than the negative threshold VRESET, the memristance returns to ROFF. If the applied voltage is in between VRESET and VSET the memristance will remain unchanged. Therefore, the memristor's two distinctive

resistance states can represent logic 0 and logic 1. The binary data can be written to the memristor through a writing voltage, and the data stored in the memristor can also be read by a small reading voltage so that the states will not be lost even if the power is off.

Fig: (a) The schematic of the memristor. (b) The qualitative current-voltage characteristic of the threshold-type switching memristor.

A. SR Flip-Flop Circuit Architecture and Operations

We proposed a memristor-based nonvolatile synchronous SR flip-flop circuit. It consists of a threshold-type memristor (ME) connected in series to a pulldown resistor (RL), two pairs of NMOS transistors (M1, M2, M3, M4), a PMOS transistor (P1), and four inverters (Inv1, Inv2, Inv3, Inv4). The set voltage is applied to S and the reset voltage is applied to R. The CP controls the switch states of M3, M4, and P1 and different transistor states can form different equivalent circuit structures to achieve different trigger functions of SR flip-flop. Compared with traditional SR flip-flop circuits, the new circuit structure is not only simpler but also has nonvolatility.

B. D Flip-Flop Circuit Architecture and Operations

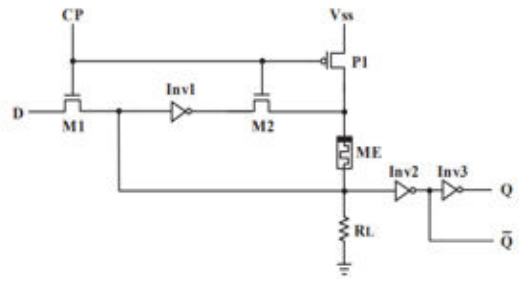


Fig 1Dlatch design

The components of the circuit include a threshold type memristor (ME), a resistor (RL), NMOS transistors (M1, M2), a PMOS transistor (P1), and inverters (Inv1, Inv2, Inv3). Its operation principles and circuit structure are similar to the SR flip-flop presented in Section II-B. When the CP is at logic 0, the M1 and M2 turn off while P1 turns on, so changes at the D input make no difference to the Q and Q^{-}. Similar to the SR flip-flop, the Q will remain unchanged. When the CP is at logic 1, then P1 turns off while M1 and M2 turn on. If the D input goes to logic 0 (logic 1), the Q is logic 0 (logic 1) since the output terminal of Q is connected to the input terminal of D. Also, the input of Inv2 is logic 0 (logic 1) and the output of Inv1 is logic 1 (logic 0), causing RME to be switched to ROFF (RON) that the Q sets to logic 0 (logic 1) when the CP changes from high to low.

CP	D	Q^n	Q^{n+1}	Characteristic
0	×	×	Q^n	Hold the state
1	0	0	0	Set to logic 0
		1	0	
	1	0	1	Set to logic 1
		1	1	

Table: Truth table of D Flip-flop

DISADVANTAGES

A. When the clock signal presents high, due to the voltage allocated on the transistors M1 and M2, usually called threshold loss, the voltage in the memristor is reduced.

B. The time for the memristor switching between different states is increased as reducing the writing voltage on the memristor will always increase the switching time of the memristor.

C. This design is not suitable for high clock frequency.

4. PROPOSED SYSTEM

We present in this section the design, analysis, and simulation results of our nonvolatile D-type latch based on a memristor that can support high clock frequency.

The structure of the proposed D latch design:

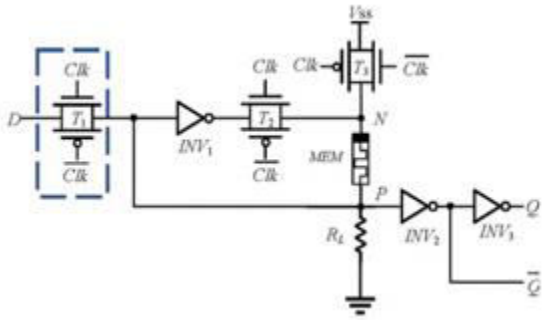


Fig 2 Proposed memistor based dflipflop

A transmission gate (the dashed box in Figure) is composed of a complementary pair of transistors and can control the transfer of logic levels from one node to another when its control signals are activated

As the threshold loss is prevented by the transmission gate, the output Q = D, which we refer to as the writing phase. When D = '0', the inverter INV1 outputs '1' at point N and the point P presents as '0'. Thus, the voltage from the positive terminal of MEM to the negative terminal of MEM equals -Vcc. As - Vcc

A. Memristor-based D Type Master-Slave Flip-Flop

In this section, we discuss how to use the above proposed memristor-based D latch to build a D master-slave flip-flop. For an enabled level-sensitive flip-flop, its content changes instantaneously when its input changes. i.e., when enabled, the input determines the output instantly. Therefore, the level-sensitive flip-flops are vulnerable

to disturbance in the input signal and cannot be widely used in large-scale digital integrated circuits. In comparison, flip-flops have their content changes only either at the rising edge or falling edge of the clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. Thus, the flip-flop is less vulnerable to noise than the latch.

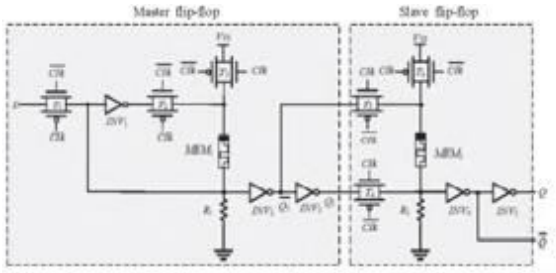
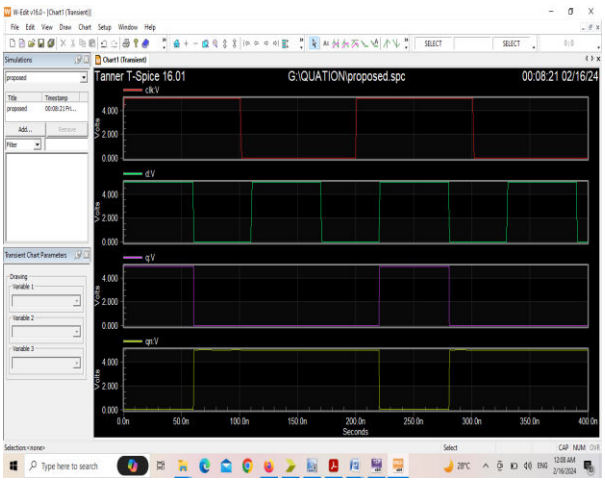


Fig 3 Memistor based flipflop design

When the Clk is low, T1, T2, and T6 are turned on while T3, T4, and T5 are turned off. The equivalent circuit is shown in Figure. The master flip-flop works in the writing phase and the input D is latched in the master flip-flop by cha

5. SIMULATION RESULT



6. CONCLUSION

As a non-volatile device, memristor has been widely explored to implement nonvolatile sequential devices so that the important data stored in memory can be immune to unexpected power failure. To enable the conventional flip-flop to be nonvolatile, it has been proposed to insert memristor between the master flip-flop and the slave flip-flop of the flipflop. In this project, we propose an improved memristor-based D-type latch and a nonvolatile flip-flop based on this new latch. The proposed latch consists of only several transmission gates, CMOS inverters and a memristor. Compared to other memristor-based latches, our design realizes a faster switching of the resistance state of the memristor, which enables the latch to support a clock of higher frequency. Also, it improves the capability of the design to resist disturbance in supply voltage. A nonvolatile master-slave DFF is

implemented based on the proposed latch. The simulation results show that the proposed DFF has advantages over existing memristor-based DFFs in terms of timing performance. In addition, its area overhead is smaller than all but one of the existing memristor-based DFF designs.

REFERENCES

[1] L. Chua, “Memristor - The missing circuit element,” IEEE Transactions on Circuit Theory, vol. 18, no. 5, January 1971, pp. 507-519

[2] B. Strukov, G. S. Snider, and D. R. Stewart, “The missing memristor found,” Nature, vol. 453, 2008, pp. 80- 83.

[3] W. Robinett, M. Pickett, and J. Borghetti, “A memristor-based nonvolatile latch circuit,” Nanotechnology, 21(23):235203, May 2010, pp. 1-6.

[4] M. Jung, K. H. Jo, and E. S. Lee, “Zero-Sleep-Leakage Flip-Flop Circuit with Conditional-Storing Memristor Retention Latch,” IEEE Transactions on Nanotechnology, vol. 11, no. 2, March 2012, pp. 360-366.

[5] I Kazi, P. Meinerzhagen, and P. E. Gaillardon, “A ReRAM-based non-volatile flip-flop with sub-VT read and CMOS voltage-compatible write,” in Proc. 2013 IEEE 11th nternational New Circuits and Systems Conference (NEWCAS), Paris, France, 2013

[6] H. Sun, X. Xu and H. Shao, “Memristor-based nonvolatile D trigger,” CN 103051307 A[P]. 2013

[7] J. Zheng, Z. Zeng and Y. Zhu, “Memristor-based nonvolatile synchronous flip-flop circuits,” in Proc. 2017 Seventh International Conference on Information Science and Technology (ICIST), Da Nang, May 2017, pp. 504- 508.

[8] MT Arafin, C Dunbar, G Qu, N McDonald, L Yan, “A survey on memristor modeling and security applications”, in Proc. 16th International Symposium on Quality Electronic Design), Santa Clara, CA, March 2015, pp. 440-447,

[9] Biolek, M. D. Ventra, and Y. V. Pershin, “Reliable SPICE simulations of memristors, memcapacitors, and meminductors,” Radioengineering, vol. 2 2, no. 4, July 2013, pp. 945-968. [10] Yakopcic, T. M. Taha, “Determining optimal switching speed for memristors in the neuromorphic system,” Electronics Letters, vol. 51, no. 21, 2015, pp. 1637-1639

[11] Harry J. M. Veendrick, Nanometer CMOS ICs: From Basics to ASICs, Springer, Heidelberg, Germany, 2008, pp. 190-191.