Advancements in Multi-Output DC-DC Converters for Electric Vehicle Integration

Mr.T.Hari Babu[1], D.Lakshmi Priyanka[2], M.SivaKumari[3], T.Manoj Kumar[4], Sk.Farook,

#1 Associate Professor in Department of EEE, in PBR VITS, KAVALI.

#2#3#4#5 B.Tech with Specialization of Electrical And Electronics Engineering in PBR Visvodaya Institute of Technology & Science , Kavali.

ABSTRACT_ In applications involving portable electronics and electric vehicles (EVs), multiport converters are crucial components. Various configurations of single-input multi-output (SIMO) converters are presented in the literature. The majority of SIMO converters provide outputs with limitations on duty ratio and inductor charging. One persistent obstacle in the design of SIMO converters is the cross-regulation issue. In this work, a SIMO topology is suggested in order to get beyond the previously described restrictions. Without regard to duty cycle or inductor current limitations, it can produce three distinct output voltages (either iL1 > iL2 > iL3 or iL1 < iL2 < iL3). Since the suggested topology does not have cross regulation issues, variations in the output current i03 (i02) (i01) have no effect on the load voltage V01 (V02) (V03). During control, the loads are separated from one another. A 200 W prototype circuit is created in the lab, and the outcomes of simulation and experimentation are confirmed.

1.INTRODUCTION

In the past decade, there has been an increase in demand for renewable energy sources utilization in electric vehicles (EVs), auxiliary power, and grid-connected applications [1]–[5]. In these applications, multiport DC-DC converters are essential for Hybridizing energy sources which lead to, reduce the components count, complexity, and cost of the system compared to several separate single input DC-DC converters [6], [7].

Over the past decade, MPC converters have been presented. A new SIMO converter is proposed in [8]. This structure simultaneously generates boost, buck, and inverted outputs controlled independently. However, producing 'n' voltage levels requires n + 2 switches, which increases the overall size and cost of the converter. Unexpected mistakes in calculating state-space equations and output voltages for a SIMO converter given in [8] are addressed and rectified in [9]. The single coupled inductor-based SIMO buck is presented in [10] with lesser output inductor current ripple than single inductor SIMO converters. Nayak and Nath [11] elaborately presented the comparative performance of SIDO converters based on the coupled inductor and single inductor (SI) in terms of cross-coupling issues. Furthermore, they proposed that the coupled inductor SIDO converter has a better steadystate and transient performance. Nevertheless, in a SI SIMO configuration inductor is switched between the loads, which causes high ripples and cross-regulation problems.

Different control approaches are proposed in the literature to overcome the cross-

regulation issue in a single inductor-based SIMO converter; the current predictor controller is presented in [12] instead of the conventional chargebalance approach. However, generating the duty ratios for active switches has been somewhat complicated. Similarly, the deadbeat-based control approach is presented in [13]. It is based on output current observer, and hence it is sensitive to the noise and significant parametric variations. In [14], a multivariable digital controller-based SIMO converter is proposed to minimize the voltage ripples, suppress the cross-regulation problems, and regulate the output voltages. However, controller design may lead to an increase in complexity

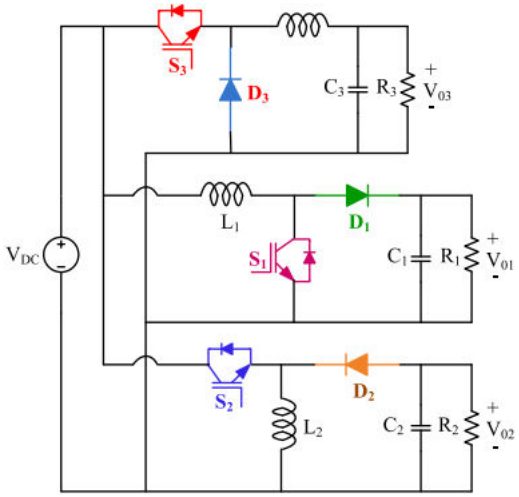


FIGURE 1. Diagram of conventional SIMO converter.

A non-secluded and single switch SIMO converter geography is introduced in [15]. It has less parts and diminishes the expense of the framework. However, it may be difficult to independently regulate the outputs.

To ease the issues in a solitary inductor SIMO converter, a non-secluded SIMO converter is proposed in [16]-[25], which are freely managed the result voltages and doesn't need an extra control circuit. In [16], another SIDO converter geography is proposed to coordinate buck and super lift converter for creating the move forward and step-down yield voltages for electrical vehicle applications. It has a limitation working proportion viz. D2 < D1, which restricts the activity scope of D1 by expanding D2. The semiconductor switches in the topologies proposed in [17] and [18] are fewer. However, the converter's operation is determined by the charging time of the inductors (iL1 > iL2). Thus, the constraint on-duty ratio remains unchanged.

The blend of high addition move forward and SEPIC converter-based SIMO is recommended for PV applications in [19]. By incorporating capacitors and diodes, this arrangement raises the voltage at both outputs above the supply voltage. By and by, the quantity of capacitors and diodes influences cost and conduction misfortunes. Another SIDO buck-help geography is created in [20] to produce positive and negative results. With fewer components, a multi-output converter is suggested in [21]. However, because it has more diodes, its conduction losses are higher. A construction of SIMO setup is presented in [22] with the benefits of decreasing the detached channel size and low voltage pressure. High-thickness multi-yield converter is proposed in [23] for compact electronic applications in light of the front-end exchanged capacitor procedure with further developed power thickness and decreased exchanging misfortunes.

Changed SEPIC and interleaved-based high move forward SIMO converter are presented in [24]. It boosts the output voltage for sustainable energy applications using a voltage multiplier, coupled inductor, and switched capacitors. In any case, it has intricacy because of additional parts. The SEPIC-Cuk converter-based four-deliberately work interleaved converter is recommended for SIMO applications in [25]. It is suitable for high-power applications with a dynamic

response and has the advantages of low ripple voltage and compact size.

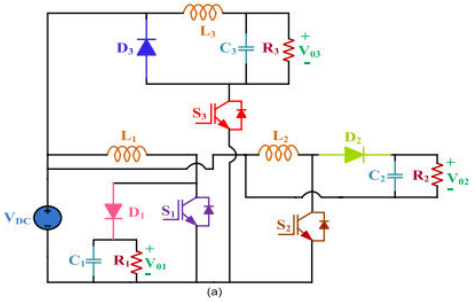
In the ordinary methodology, EVs' assistant power supply framework to deal with the heap prerequisites is displayed in Figure 1. Although it appears straightforward, the primary drawback of this strategy is a cross-regulation issue and the fact that the loads are not isolated from one another during their operation. When simultaneously charging the battery with turn-on loads and if the ground is involved, there is also the possibility of grounding issues. In addition, converting one of the negative output voltages into buck-boost operation mode will increase the complexity of the circuit.

The onboard power converter is the primary focus of the investigation in the proposed work. The configuration of the circuit in Figure 2(a) ensures that the energy stored in the inductor is restricted to just one output and is not shared with the other outputs during control, enabling independent duty-cycle regulation of the output voltages. All the more critically, the heaps are detached from one another during control, and the cross-guideline issue is effectively wiped out. Additionally, since it is an onboard power converter, grounding poses no problems even when battery charging and grounding are involved.

2.PROPOSED WORK

Figure 2(a) shows the suggested single input, three-output DC-DC design. The parts of this design are as follows: passive elements (L1-C1, L2-C2, and L3-C3), switches (S1-S3), diodes (D1-D3), and input voltage VDC. Three distinct output voltages can be produced by it: buck (V03), buck-boost (V02) with positive voltage polarity, and boost (V01). The duty cycles D1, D2, and D3, respectively, can be used to independently regulate the output voltages with the suggested converter. Figure 2(b) shows the theoretical waveforms of circuit elements.

The traditional parallel combination of buck, boost, and buck-boost configuration is not the same as the suggested setup. The loads in the suggested circuit configuration are isolated while the control is happening simultaneously. As can be seen from the accompanying pictures, load R3 through S3 alone is linked to the input power supply during mode-1 operation, while the remaining loads are separated, as Figure 3(a) illustrates. Similarly, as shown in Figure 3(b), only load R1 through D1 is linked to the input supply during mode-2; all other loads are isolated. Every load in the suggested control strategy is kept apart from the others while it is being controlled in any mode of operation. But this feature is unattainable.



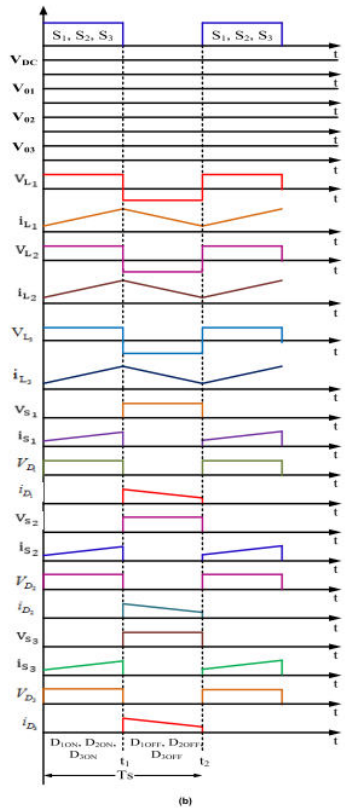


FIGURE 2. Proposed configuration: (a) SIMO configuration,(b) Theoretical waveforms.

in the buck, boost, and buck-boost converter combinations used in normal parallel operation. Despite its apparent simplicity, this circuit arrangement is unique and useful. Table 1 presents a comparison between the traditional and proposed SIMO converters with respect to their component counts, modes of operation, and working circumstances.

TABLE 1. Parameter specification comparison between the conventional and proposed SIMO converter.

Comparison different aspects	Conventional	Proposed
Number of components	6	6
Output voltage	Buck, Boost, and Buck-Boost **(Negative output voltage)**	Buck, Boost, and Buck-Boost **(Positive output voltage)**
Inverting circuit is required for the positive output voltage	Yes	No
Loads are isolated to each other during control	No	Yes

In the conventional approach shown in Figure1, the main drawback is the cross-regulation problem, and the loads are not isolated from each other during their operation. Further, the circuit complexity will increase to convert the negative polarity of output voltages in the buck-boost mode of operation.

The proposed structure has the following advantages:

a) It is a simple structure and no assumptions on operating

duty ratio (D1 > D2 > D3 or D3 < D2 < D1 or D1 = D2 = D3)

b) It can generate three different output voltages, i.e.,boost, buck, buck-boost()

c) No constraints on inductor currents (like iL1 > iL2 >iL3 or iL1 < iL2 < iL3 or iL1 = iL2 = iL3)

d) Loads are isolated from each other during control and the cross-regulation problem is successfully eliminated

e) It gives the positive buck-boost output voltage

A. MODES OF OPERATION

1) SWITCHING STATE 1

Switches S1, S2, and S3 are turned ON. The current flow path is depicted in Figure 3(a), and the energy port VDC magnetizes L1, L2, and L3. Consequently, the C1 and C2 are discharged to the loads (R1) and (R2), respectively, whereas (C3) is

charged. The inductor currents and capacitor voltages are represented in Eq. (1)-(4).

$$i_{L_1}(t) = \frac{V_{DC}}{L_1}t + i_{L_1(0)}, \quad v_{C_1}(t) = v_{C_1(0)}e^{\frac{-1}{R_1C_1}t}$$

$$i_{L_2}(t) = \frac{V_{DC}}{L_2}t + i_{L_2(0)}, \quad v_{C_2}(t) = v_{C_2(0)}e^{\frac{-1}{R_2C_2}t}$$

$$i_{L_3}(t) = \frac{V_{DC}}{R_3} + e^{-\alpha t}\left[c_1\cos\omega_d t + c_2\sin\omega_d t\right]$$

$$v_{C_3}(t) = V_{DC} - \frac{L_3}{2C_3}e^{-\alpha t}\begin{bmatrix}\cos\omega_d t(\frac{\alpha c_1}{R_3} + \omega_d c_2)\\ +\sin\omega_d t(-\alpha c_2 + \frac{\omega_d c_1}{R_3})\end{bmatrix}$$

2) SWITCHING STATE 2

In this state, L1, L2, and L3 are de-magnetized and deliver their energy to the load through D1, D2, and D3, respectively.

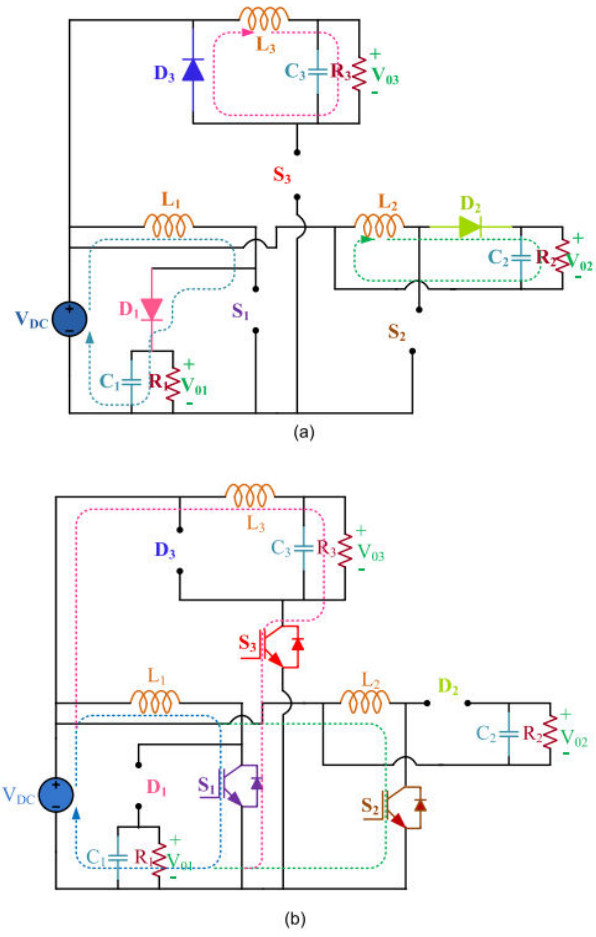


FIGURE 3. Operating states: (a) Switching state-1 and (b) Switching state-2.

It is illustrated in Figure 3(b). The inductor currents and capacitor voltages are in Eq. (5)–(11) as follows,

$$i_{L_1}(t) = \frac{V_{DC}}{R_1} + e^{-\alpha_1 t}\left[c_1\cos\omega_{d1}t + c_2\sin\omega_{d1}t\right] \quad (5)$$

$$v_{C_1}(t) = V_{DC} - \frac{L_1}{2C_1}e^{-\alpha_1 t}\begin{bmatrix}\cos\omega_{d1}t(\frac{c_1}{R_1} - \omega_{d1}c_2)\\ +\sin\omega_{d1}t(\omega_{d1}c_1 + \frac{c_2}{R_1})\end{bmatrix} \quad (6)$$

$$i_{L_2}(t) = e^{-\alpha_2 t}\left[c_3\cos\omega_{d2}t + c_4\sin\omega_{d2}t\right] \quad (7)$$

$$v_{C_2}(t) = -L_2e^{-\alpha_2 t}\begin{bmatrix}(-\alpha_2 c_3 + \omega_{d2}c_4)\cos\omega_{d2}t\\ +(\omega_{d2}c_3 - \alpha_2 c_4)\sin\omega_{d2}t\end{bmatrix} \quad (8)$$

$$i_{L_3}(t) = e^{-\alpha t}\left[c_5\cos\omega_d t + c_6\sin\omega_d t\right] \quad (9)$$

$$v_{C_3}(t) = -L_3e^{-\alpha t}\begin{bmatrix}(-\alpha c_5 + \omega_d c_6)\cos\omega_d t\\ +(\omega_d c_5 - \alpha c_6)\sin\omega_d t\end{bmatrix} \quad (10)$$

$$\alpha_1 = \frac{1}{2R_1C_1}, \quad \omega_{d1} = \frac{1}{2}\sqrt{\left(\frac{1}{R_1^2C_1^2} - \frac{4}{L_1C_1}\right)},$$

$$\alpha_2 = \frac{1}{2R_2C_2} \quad \text{and } \omega_{d2} = \frac{1}{2}\sqrt{\left(\frac{1}{R_2^2C_2^2} - \frac{4}{L_2C_2}\right)}$$

$$\alpha = \frac{1}{2R_3C_3}, \quad \omega_d = \frac{1}{2}\sqrt{\left(\frac{1}{R_3^2C_3^2} - \frac{4}{L_3C_3}\right)}, \quad (11)$$

where c1, c2, c3, c4, c5, and c6 areinitial values.

Output voltages of the proposed configuration are as follows

$$V_{01} = \frac{V_{DC}}{(1-D_1)}, \quad V_{02} = \frac{V_{DC}D_2}{(1-D_2)}, \; V_{03} = D_3V_{DC} \quad (12)$$

D1, D2, and D3 are duty ratios of the S1, S2, and S3 respectively.

As seen in Figure 3(a), it is seen that load (R3) alone through S4 is linked to the ground during switching state-1 operation, while the other loads are segregated even when the earth is involved during battery charging. Similar to this, only load (R1) through D1 is linked to the ground during switching state-2; other loads, as shown in Figure 3(b), are isolated from both the ground and load (R1). Every load in the suggested control strategy is kept apart

from the others while it is being controlled in any mode of operation.

Additionally, the circuit's design ensures that the inductor's stored energy is limited to a single output and is not shared with any other outputs during control. This permits separate duty-cycle regulation of the output voltages. Consequently, the fluctuation in load current i03 (i02) (i01) has no effect on the load voltage V01 (V02) (V03). Hence, even in cases when the ground is engaged during battery charging, the suggested setup using this control method eliminates all crossregulation difficulties. More significantly, the arrangement is straightforward and allows for the generation of three independent outputs without any assumptions about operating duty cycle or inductor currents (iL1 = iL2 = iL3 or iL1 < iL2 < iL3).

B. SEMICONDUCTOR STRESS ANALYSIS

Semiconductor stresses of the proposed configuration are presented Eq. (13)-(15) as [27].

1) VOLTAGE STRESSES

$$V_{S_1} = V_{01}, \quad V_{D_1} = V_{01}, \; V_{S_2} = \left(\frac{V_{02} + V_{DC}}{2}\right)$$
$$V_{D_2} = (V_{02} + V_{DC}), \quad S_3 = V_{D_3} = V_{DC} \qquad (1$$

2) CURRENT STRESSES

a: MODE 1

$$i_{S_1} = i_{L_1}, \quad i_{D_1} = 0, \; i_{S_2} = i_{L_2},$$
$$i_{D_2} = 0, \quad i_{S_3} = i_{L_3}, \; i_{D_3} = 0 \qquad (14)$$

b: MODE 2

$$i_{S_1} = i_{D_1} = i_{L_1}, \quad i_{S_2} = i_{S_3} = 0,$$
$$i_{D_2} = i_{L_1}, \quad i_{D_3} = i_{L_3} \qquad (15)$$

III. SMALL-SIGNAL MODELING

The transfer function of the proposed topology is derived from small signal analysis as [26]. The state-space equations (16)-(25) are as follows

$$[A]\,X(t) = Bx(t) + Cu(t) \qquad (16)$$
$$y(t) = Dx(t) + Eu(t) \qquad (17)$$

$$\frac{d}{dt}\begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ i_{L_3}(t) \\ v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \end{bmatrix} = B\begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ i_{L_3}(t) \\ v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \end{bmatrix} + CV_{DC} \qquad (18)$$

$$B = \begin{bmatrix} 0 & 0 & 0 & -\left(\frac{1-D_1}{L_1}\right) & 0 & 0 \\ 0 & 0 & 0 & 0 & \left(\frac{1-D_2}{L_2}\right) & 0 \\ 0 & 0 & 0 & 0 & 0 & \left(\frac{1-D_3}{L_3}\right) \\ \left(\frac{1-D_1}{C_1}\right) & 0 & 0 & \frac{-1}{R_1C_1} & 0 & 0 \\ 0 & \left(\frac{1-D_2}{C_2}\right) & 0 & 0 & \frac{-1}{R_2C_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_2C_2} \end{bmatrix} \qquad (19)$$

$$C = \begin{bmatrix} \frac{1}{L_1} \\ \frac{D_2}{L_2} \\ \frac{D_3}{L_3} \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad (20)$$

$$D = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \qquad (21)$$

where state-space coefficients are A, B, C, D and E X(t) =state vector, U(t) = input vector, and y(t) = output vector

Where, State vector = x(t), Input vector = u(t) and Output vector = y(t). (18)–(21), as shown at the bottom of the next page.

The output voltages $V\hat{}_{01}$ $V\hat{}_{02}$ and $V\hat{}_{03}$ are determined by $d\hat{}_1$and $d\hat{}_2$, and $d\hat{}_3$

$$\hat{v}_{01}(s) = G_{vd1}\hat{d}_1(s), \hat{v}_{02}(s) = G_{vd2}\hat{d}_2(s),$$
$$\hat{v}_{03}(s) = G_{vd3}\hat{d}_3(s) \qquad (22)$$

The proposed configuration control transfer function is given in Eq. (23-25) as follows

$$\frac{\hat{v}_{01}(s)}{\hat{d}_1(s)} = \frac{V_{DC}}{(1-D_1)^2}\left[\frac{1 - s\frac{L_1}{R_1(1-D_1)^2}}{1 + s\frac{L_1}{R_1(1-D_1)^2} + s^2\frac{L_1C_1}{(1-D_1)^2}}\right]$$

$$\frac{\hat{v}_{02}(s)}{\hat{d}_2(s)} = \frac{V_{DC}}{(1-D_2)^2}\left[\frac{1 - sD_2\frac{L_2}{R_2(1-D_2)^2}}{1 + s\frac{L_2}{R_2(1-D_2)^2} + s^2\frac{L_2C_2}{(1-D_2)^2}}\right]$$

$$\frac{\hat{v}_{03}(s)}{\hat{d}_3(s)} = V_{DC}\left[\frac{1}{1 + s\frac{L_3}{R_3} + s^2L_3C_3}\right]$$

The bode plot of the proposed configuration is illustrated in Figure 4 for verifying the stability. It is observed that the gain margin is 6.65 dB, 1.54 dB, and −1.55 dB, whereas the phase margin is 90◦ and 90◦ and 0.393◦ respectively for transfer functions of the proposed converter given in (23)-(25).

IV. CONTROLLER DESIGN, PARAMETER DESIGN,SMALL-SIGNAL MODELING, POWER LOSSES CALCULATIONS, AND COMPARATIVE ASSESSMENT

A. THE CONTROL METHOD OF THE PROPOSED CONVERTER

A suitable control scheme is essential for good voltage regulation. A control transfer function has been derived for each output by using small-signal modeling. It is cascaded with a controller, as illustrated in Figure 5, where the PI-controller is chosen as given (26) to reduce the undamped behavior of the system and improve the low-frequency performance, i.e.,it reduces the steady-state error [18].

$$G_{c1}(s) = \left(\frac{K_P s + K_I}{s}\right), \quad G_{c2}(s) = \left(\frac{K_P s + K_I}{s}\right),$$

$$G_{c2}(s) = \left(\frac{K_P s + K_I}{s}\right)$$

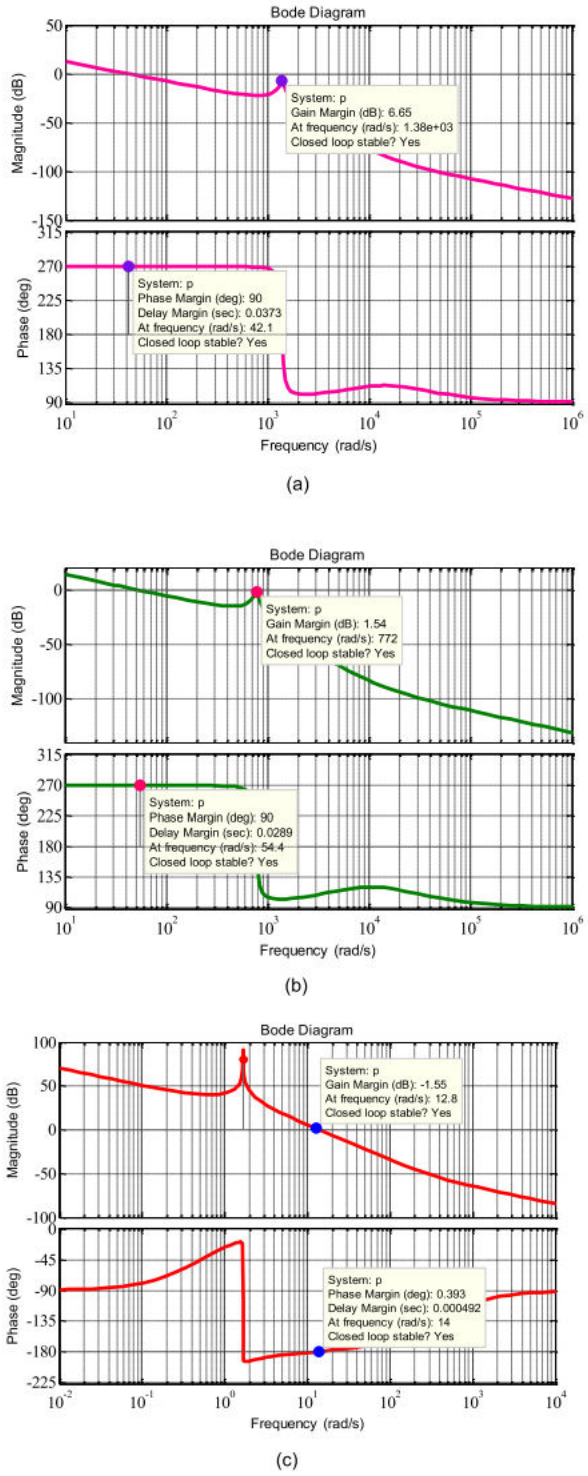


FIGURE 4. Bode plot of the proposed converter.

B. PARAMETERS DESIGN CONSIDERATIONS

The converter parameters design can be calculated using equations (27)-(29) as given in [27].

$$L_{1\min} = L_{2\min} = \frac{2}{27}\frac{R_{L\max}}{f_s}, \quad L_{3\min} = \frac{R_{L\max}(1 - D_{\min})}{2f} \tag{27}$$

fs = switching frequency, Dmin = Minimum duty cycle

Calculation of filter capacitance value is

$$C_{1\min} = \frac{D_{\max}V_{01}}{V_{cpp}R_{L1\max}f_s}, \quad C_{2\min} = \frac{D_{\max}V_{02}}{V_{cpp}R_{L2\max}f_s}, \quad C_{3\min} = \frac{D_{\max}}{2r_cf_s} \tag{28}$$

where

V01,02,03 = Output voltage, Dmax = Maximum duty ratio, fs = Switching frequency, RL1,2max = Maximum load resistance, rc = Maximum ESR of thefilter capacitor and Vcpp =Peak-to-peak value of the capacitor.

$$V_{cpp} = \frac{V_r}{2} \tag{29}$$

The ripple voltage (Vr) is 1% of V0

C. POWER LOSSES CALCULATIONS

Power losses are essential for calculating efficiency as follows [28], [29], equations are presented in Eq. [30]–[35]

$$P_{loss\_IGBT} = P_{con} + P_{sw} \tag{30}$$

TABLE 2. Parameter specifications.

Parameter	Simulation	Experimental
Input voltage (V_{DC})	50 V	50 V
Output voltage ($V_{01}/V_{02}/V_{03}$)	100/50/25 V	100/50/25 V
Output currents ($I_{01}/I_{02}/I_{03}$)	2/2/2 A	2/2/2 A
Switching frequency (f)	50 kHz	50 kHz
Inductor ($L_1/L_2/L_3$)	0.6/0.9/1 mH	0.5/1/1 mH
Capacitor ($C_1/C_2/C_3$)	200/470/360 uF	220/470/470 uF

The IGBT conduction losses are

$$P_{con} = \frac{1}{T}\int_0^T (R_{on}i_F + V_{Fo})i_F dt \tag{31}$$

Ron = Switch ON-state resistance, VFo = Threshold voltage, iF = Forward current, and T = Switching period.

The switching losses are calculated as,

$$P_{sw} = (E_{OFF,j} + E_{ON,j}) \times f \tag{32}$$

where EON and EOFF are and is the energy delivered in ON and OFF time of the power switches, respectively, and f is the switching frequency

$$P_L = r_L I_{Lrms}^2, I_{Lrms} = \frac{I_0}{(1 - D)} \tag{33}$$

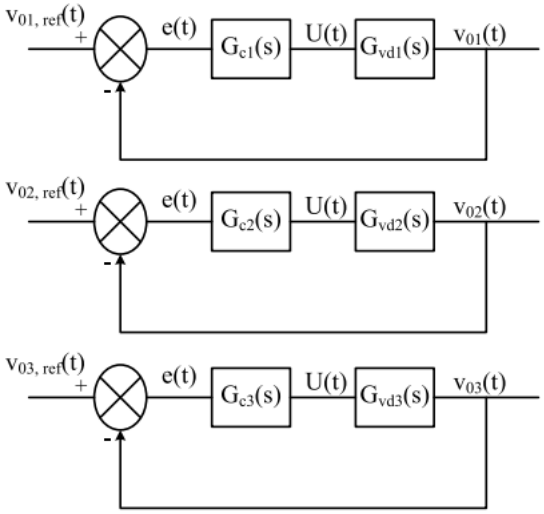


FIGURE 5. Closed-loop control system.

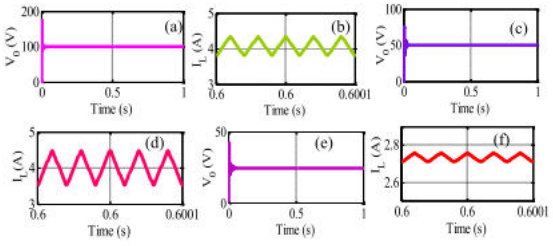


FIGURE 6. (a) V_{01}, (b) i_{L1}, (c) V_{03}, (d) i_{L2}, (e) V_0, (f) iL_3.

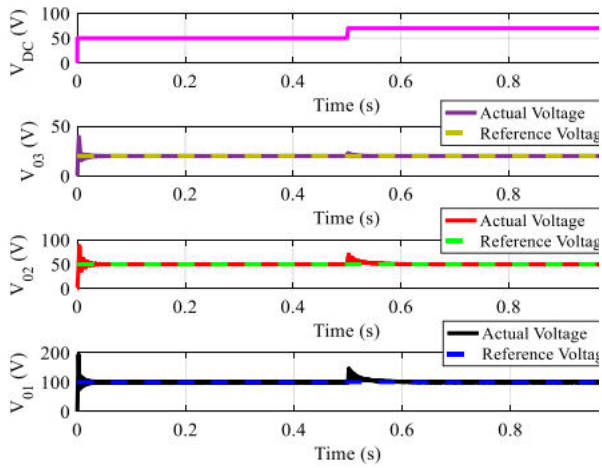


FIGURE 7. Performance of closed-loop control for a sudden variation in input voltage (VDC) at 0.5 sec.

The power loss of the capacitor (PC) is calculated as

$$P_C = r_C I_{Crms}^2, I_{Crms} = I_0 \sqrt{\frac{D}{(1-D)}} \quad (34)$$

where ILrms is the RMS value of the inductor current and ICrms RMMMS values of the capacitor current. rC, and rL are the ESR of the capacitor and inductor, respectively.

The efficiency of the proposed converter is

$$\eta = \frac{P_{out}}{P_{out} + P_{sw} + P_{con} + P_L + P_C} \quad (35)$$

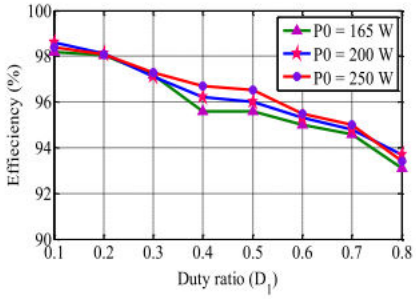


FIGURE 8. The efficiency of the proposed topology at different duty ratios.

FIGURE 9. Experimental results: (a) V01, (b) iL1, (c) I01, (d) V02, (e) (iL2),(f) (I02), (g) V03, (h) (iL3) and (i) (I03).

D. COMPARATIVE ASSESSMENT

The comparative assessment is presented in this section in terms of components, passive elements, and stresses on active switches for recently developed SIMO DC-DC converters in the literature.

1) THE NUMBER OF COMPONENTS

The comparative assessment based on the number of components has been done with recently reported single input multi output topologies as depicted in Table. 3. A single switch SIMO converter is presented in [15]; it reduces the control complexity of the system. Nevertheless, it may not be easy to regulate the outputs independently. A SIDO configuration is developed in [16] using a super-lift Luo-converter. It generates both step-up and step-down outputs. However, it has more components count. Reference [20] observed that the presented SIMO generates positive and negative output voltages. However, it increases the number of components that result in big size, high cost, and more power losses. The proposed converter in [18] has reduced part count and is suitable for EV auxiliary power supply

applications. Nevertheless, it has such as iL1 > iL2 for generating output voltages. In [21], a multi-output converter is developed with reduced components. Nevertheless, it may have high conduction losses due to more diodes. A new SIDO topology is

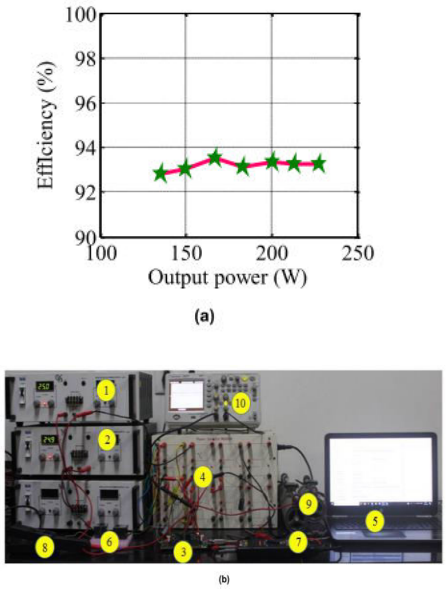


FIGURE 10. (a) Efficiency of the proposed configuration, (b) Experimental setup developed in the laboratory: (1), (2) Voltage sources, (3) DSP 28335 Controller, (4) IGBT Module, (5) Host PC, (6),Inductor (L1, L2), (7) Differential probe, (8) Current probe, (9) Load (R), (10) DSO.

presented in [22] has the advantages of low semiconductor stress and the size of the filter elements. However, it has more device count, which may affect the size of the power converter. A high-density multioutput converter is suggested in [23] for portable electronic applications, has more active switches, which may decrease the converter efficiency.

The comparison presented in Table 3 depicts that the proposed configuration is simple, and there are no assumptions on the inductor currents and operating duty ratio. It can generate three independent outputs and loads are isolated from each other during control and the cross-regulation problem is successfully eliminated.

2) VOLTAGE STRESS COMPARISON

The efficacy of the proposed configuration is also compared in terms of the voltage stress and is shown in Table 2. The maximum voltage stress of the proposed topology in [20] is the addition of input and output voltage. Similarly, topologies introduced in [18] and [22] have less voltage stress, i.e., half of the output voltage and supply voltage. The proposed configuration in [16] is the subtraction of output and supply voltage. The maximum voltage stress in the presented topology in [15] and proposed configuration is the output voltage. The suggested topology in [23] has low semiconductor stress. From Table 2, one can observe that the proposed topology has less semiconductor stress compared to suggested topologies in [16], [18], and [22]. The current stress on the switch is high in the presented topologies [18], and [20] is equal to the addition of inductor current. The proposed topology and converter proposed in [15], [16], [22], and [23] have less current stress, i.e., current flows through the one inductor (iL2) only.

The proposed converter's comparative analysis has also been done in terms of control complexity and power density, as depicted in Table 4. The control complexity and power density are mainly dependent on the number of active switches and the total number of components in the power converter. It is observed that the topologies proposed in [19], [20], and [21] have a lesser number of active power switches as compared with [18], [22], [23], and the proposed topology. Hence they had low complexity in control. Similarly, the power density of any DC-DC converter mainly depends on the total number of components, especially active power switches, and they occupy more space. Consequently, the proposed power converter and topologies presented

in [18], [20], and [22] have higher power densities.

Moreover, with the comparison of different aspects of power converter such as component count, semiconductor stresses, from Table. 2 suggests that each converter has its own merits and demerits. The proposed converter structure has low semiconductor stresses and avoids cross-regulation problems if the ground is involved during the charging of the input battery. The configuration is suitable for EVs' auxiliary power system applications.

4. RESULTS AND DISCUSSIONS

A. SIMULATION RESULTS

The model has been built in MATLAB environment to verify the proposed system with VDC = 50 V, frequency is 50 kHz, and the duty ratio is 50%. The parameter details are specified in Table. 2. The corresponding output voltages (V01,V02, and V03) and inductor currents (iL1, iL2, and iL3) are illustrated in Figure 6(a-f), respectively. The output voltages in Figures 6(a), 6(c) 6(e) are close to the theoretical results. The closed-loop control is implemented for the proposed configuration, and the dynamic performance of the overall system is validated for a sudden change in the input voltage. Figure 7. shows the simulation result of closed-loop control for a sudden change in the input voltage (VDC) from 50V to 70 V at 0.5 sec. The PI control gains are chosen as Kp =0.1 and Ki = 15 for Buck output, similarly Kp = 0.005 and Ki = 0.5 for Boost and Buck-Boost voltages.

TABLE 3. Comparison between different SIMO topologies.

Ref.	G_{pot}	$S_{V\_stress}/S_{I\_stress}$	$D_{V\_stress}/D_{I\_stress}$	N_S	N_D	N_L	N_C	$N_{comp.}$	N_{sup}	N_{capa}	Loads are isolated from each other during control
[15]	$V_{01}=\frac{D}{(1-D)}$, $V_{02}=\frac{1}{(1-D)}$, $D<1$	$V_{Smax}=V_{02}$, $i_{Smax}=i_{L_1}$	$V_{Dmax}=V_g+V_{01}$, $i_{Dmax}=i_{L_2}$	1	2	2	3	8	1	2	Yes
[16]	$V_{01}=\frac{V_{in}(2-D_2)}{(1-D_2)}$, $V_{02}=\frac{V_{in}(D_1-D_2)}{(1-D_2)}$, $D_2<D_1$	$V_{Smax}=V_{01}-V_{in}$, $i_{Smax}=I_{in}-I_{01}$	$V_{Dmax}=V_{01}-V_{in}$, $I_{Dmax}=I_{01}$	2	3	2	3	10	1	2	Yes
[18]	$V_{01}=D_1V_i$, $V_{02}=D_2V_i$, $D_1+D_2<1$	$V_{Smax}=V_i$, $V_{S_{(1-2}}=V_i$, $i_{Smax}=i_{L_1}+i_{L_2}$		3	-	2	2	7	1	2	Yes
[20]	$V_{01}=\frac{V_{in}D}{(1-D)}$, $V_{02}=\frac{-V_{in}D}{(1-D)}$, $0<D<1$	$V_{Smax}=V_{in}+V_{02}$, $i_{Smax}=i_{L_1}+i_L$	$V_{Dmax}=V_{in}+V_{02}$, $V_{Dmax}=V_{01}-V_{02}$	2	3	2	3	10	1	2	Yes
[22]	$v_{01}=\frac{v_{in}}{(2-d_1-d_2)}$, $v_{02}=\frac{v_{in}(1-d_2)}{(2-d_1-d_2)}$, $0.5<d_1$ & $d_2<1$	$V_{Smax}=\frac{V_{01}}{2}$, $i_{Smax}=i_{L_1}$		6	-	2	3	11	1	2	Yes
[23]	$V_{01}=\frac{2+D}{3}$, $V_{02}=\frac{1+D}{3}$, $V_{03}=\frac{D}{3}$, $0<D<1$	$V_{Smax}=V_{01}$, $i_{Smax}=i_{L_1}$		12	-	3	8	23	1	3	Yes
Proposed	$V_{01}=\frac{V_{DC}}{(1-D_1)}$, $V_{02}=\frac{D_2V_{DC}}{(1-D_2)}$, $V_{03}=D_3V_{DC}$, $0<D_1<1, 0<D_2<1$, $0<D_3<1$	$V_{Smax}=V_{01}$, $i_{Smax}=i_{L_1}$	$V_{Dmax}=V_{01}$, $i_{Dmax}=i_{L_1}$	3	3	3	3	12	1	3	No

TABLE 4. Comparison of complexity, power density, and efficiency.

Ref.	Complexity		Power density	
	Power switches	Complexity in controller design	Total number of components	Power dens each topo
20	S=2	Less	10	High
19	S=1	Less	24	Low
18	S=3	Less	7	High
21	S=2	Less	18	Low
22	S=4	Less	11	High
23	S=12	High	23	Low
Proposed	S=2	Less	12	High

The results show that the proposed configuration generates stiff independent output voltages and is not affected by the sudden change in supply. The efficiency of the proposed converter at different duty ratios and various power ratings is depicted in Figure 8.

3.CONCLUSION

The structure of the SIMO converter is proposed in this paper. The operating principle and modes of operation have been explained in detail. The proposed configuration is simple and without assumptions on the charging of inductors and operating duty cycle. It can generate the buck, boost, and buck-boost output voltages with independent regulated voltages. Cross regulation problems do not

exist in the proposed topology, so the sudden change in inductor and load currents does not affect the output voltages. Finally, simulation and experimental results validate the proposed converter operation and performance.

REFERENCES

[1] P. C. Heris, Z. Saadatizadeh, and E. Babaei, ‘‘A new two input-single output high voltage gain converter with ripple-free input currents and reduced voltage on semiconductors,’’ IEEE Trans. Power Electron., vol. 34, no. 8, pp. 7693–7702, Aug. 2019, doi: 10.1109/TPEL.2018.2880493.

[2] A. Farakhor, M. Abapour, and M. Sabahi, ‘‘Design, analysis, and implementation of a multiport DC–DC converter for renewable energy applications,’’ IET Power Electron., vol. 12, no. 3, pp. 465–475, Mar. 2019.

[3] S. K. Mishra, K. K. Nayak, M. S. Rana, and V. Dharmarajan, ‘‘Switchedboost action based multiport converter,’’ IEEE Trans. Ind. Appl., vol. 55, no. 1, pp. 964–975, Jan./Feb. 2019.

[4] X. Lu, K. L. V. Iyer, C. Lai, K. Mukherjee, and N. C. Kar, ‘‘Design and testing of a multi-port sustainable DC fast-charging system for electric vehicles,’’ Electr. Power Compon. Syst., vol. 44, no. 14, pp. 1576–1587, Aug. 2016.

[5] E. Babaei and O. Abbasi, ‘‘A new topology for bidirectional multi-input multi-output buck direct current–direct current converter,’’ Int. Trans. Electr. Energ. Syst., vol. 27, no. 2, pp. 1–15, Feb. 2017.

[6] Z. Rehman, I. Al-Bahadly, and S. Mukhopadhyay, ‘‘Multiinput DC–DC converters in renewable energy applications—An overview,’’ Renew. Sustain. Energy Rev., vol. 41, pp. 521–539, Jan. 2015.

[7] G. Chen, Y. Liu, X. Qing, and F. Wang, ‘‘Synthesis of integrated multi-port DC–DC converters with reduced switches,’’ IEEE Trans. Ind. Electron.,vol. 67, no. 6, pp. 4536–4546, Jun. 2019.

[8] P. Patra, A. Patra, and N. Misra, ‘‘A single-inductor multiple-output switcher with simultaneous buck, boost, and inverted outputs,’’ IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1936–1951, Apr. 2012.

[9] M. Abbasi, A. Afifi, and M. R. A. Pahlavani, ‘‘Comments on ‘a singleinductor multiple-output switcher with simultaneous buck, boost, and inverted outputs,’’’ IEEE Trans. Power Electron., vol. 34, no. 2, pp. 1980–1984, Feb. 2019.

[10] Y.-C. Hsu, J.-Y. Lin, C.-H. Wang, and S.-W. Chou, ‘‘An SIMO stepdown converter with coupled inductor,’’ in Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT), Hsinchu, Taiwan, Aug. 2020, pp. 1–4, doi: 10.1109/VLSI-DAT49148.2020.9196435.

Author’s Profiles

Mr.T.Hari Babuworking as Associate Professor in Department of EEE, PBR Visvodaya Institute of Technology and Science KAVALI.

Team Members

D.Lakshmi Priyanka B.Tech with Specialization of Electrical And Electronics Engineering in PBR Visvodaya Institute of Technology & Science, Kavali.

T.Manoj KumarB.Tech with Specialization of Electrical And Electronics Engineering in PBR Visvodaya Institute of Technology & Science, Kavali.

M.SivaKumariB.Tech with Specialization of Electrical And Electronics Engineering in PBR Visvodaya Institute of Technology & Science, Kavali.

SK.Farook B.Tech with Specialization of Electrical And Electronics Engineering in PBR Visvodaya Institute of Technology & Science, Kavali.