A NOVEL 18T HYBRID TOPOLOGICAL FLIP-FLOP DESIGN FOR LOW POWER APPLICATION

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ABSTRACT: Flip flop are basic storage elements used extensively in digital system designs, which adopt intensive pipelining techniques and employ several FF-rich modules such as register files, shift registers, and FIFO. The power consumption of the FFs employed in a typical digital system design, along with that of clock distribution networks In this project, an ultralow-power true single-phase clocking flip-flop (FF) design achieved using only 19 transistors is proposed. The design follows a master–slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and complementary pass-transistor logic. In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. In this design, a virtual *V*DD design technique, which facilitates a faster state transition in the slave latch, is devised to enhance time performance. In circuit implementation, transistor sizes are optimized with respect to the power delay product (PDP).

INTRODUCTION

In electronics, flip-flops and latches are circuits that have two stable states that can store state information – a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will output its state (often along with its logical complement too). It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements to store a single *bit* (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of *state*, and such a circuit is described as

sequential logic in electronics. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

The term flip-flop has historically referred generically to both level-triggered (asynchronous, transparent, or opaque) and edge-triggered (synchronous, or clocked) circuits that store a single bit of data using gates. Modern authors reserve the term *flip-flop* exclusively for edge-triggered storage elements and *latches* for level-triggered ones.The terms "edge-triggered", and "level-triggered" may be used to avoid ambiguity

In the era of big data, data protection is vital and challenging because no one can predict where and when the next downtime will occur. Data backup technology is one of the best solutions in practice to minimize data loss and other negative impacts. Therefore, the efficiency in data backup and restoring will determine whether the system can maintain a continuous and stable operation. During the backup process, data stored in the volatile memory will be transferred to the nonvolatile memory and restored after downtime ends. The latency for the data transportation mainly depends on the type of memory and the structure of the system. How to minimize such latency becomes crucial for the efficiency of data backup. Flip-flops and latches are the fundamental building blocks of digital electronic systems. Traditional flip-flops are volatile memory and will lose the data they store in case of a power interrupt. Many techniques have been proposed to implement the maintenance of the intermediate state of flip-flops. One interesting approach that recently gains a lot of attention is to exploit various emerging memory technologies, including ferroelectric RAM, phase change RAM, spin-transfer torque magnetic RAM, and ferroelectric transistor, to maintain the volatile content in flip-flops for data backup and restoration operations.

They have the best transfer speed with high cost per bit, both in device area (6 transistors, 6T) and financial. In the next tier are the dynamic random-access memories (DRAMs), used for main memory. These memories need constant refreshes to maintain the data, so it generates more heat than the SRAMs but are much smaller (1T1C, 1 capacitor) and cheaper. Disk drives and NAND-based solid-state storage drives (SSDs) are used for storage. In the last tier are the hard disk drives (HDD). Both these

categories are very slow, but cheap, so usually they have the biggest storage capacity in terms of bytes.

The low-power redundant-transition-free TSPC dual-edge-triggering flip-flop using single-transistor-clocked buffer was proposed by Zisong Wang, Peiyi Zhao, and the rest of their research team at the Fowler School of Engineering, Chapman University, Orange, CA 92866, USA.

In coming days, Power consumption is major concern in digital electronics. Based on digital electronics microprocessors and micro-controller chips are major role. If we can reduce power consumption in these chips then overall device power consumption is decreases.

In modern high-performance processors, flip-flops are one of the major sources of power consumption. This is because FFs are constantly switching to capture data at the rising and falling edges of the clock signal. To reduce the power consumption of FFs, a number of low-power FF designs have been proposed.

The Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop, employing a Single-Transistor-Clocked Buffer, represents a sophisticated circuit design aimed at minimizing power consumption and enhancing reliability in digital systems. This innovative flip-flop leverages dual-edge triggering for efficient signal processing while strategically integrating a single-transistor clocked buffer to optimize power efficiency. The redundancy elimination ensures a smooth transition between states, contributing to the overall reliability of the flip-flop. This introduction sets the stage for a comprehensive exploration of the features and advantages inherent in this cutting-edge circuit design, especially when facing the drive from modern graphics processing unit (GPU)/artificial intelligence (AI) neural network processors. The computing power used in AI training has doubled every 3.4 months.

2.LITERATURE SURVEY

H.Kawaguchi and T.Sakurai, A decreased clock-swing flip-tumble (RCSF) for 63% power reduction.A diminished clock-swing flip-slump (RCSFF) is proposed, which is made out of a lessened swing clock driver and an uncommon flip-flounder which typifies the release momentum cutoff component. The RCSFF can decrease the clock framework energy of a VLSI down to 33% contrasted with the traditional flip-flounder. This power change is accomplished through the lessened clock swing down to 1 V. The zone and the

postponement of the RCSFF can likewise be diminished by a factor of around 20% contrasted with the ordinary flipflop. The RCSFF can likewise diminish the RC postponement of a long RC interconnect to one-half.

V.Oklobdzija, V.Stojanovic, D.Markovic, and N.Nedovic, Digital System Clocking High-Performance and Low-Power Aspects .In CMOS multistage clock cradle plan, the obligation cycle of clock is at risk to be changed when the clock goes through a few cushion stages. The beat width might be changed because of unbalance of the p-and nMOS transistors in the long cradle. This paper depicts a deferral bolted circle with twofold edge synchronization for use in a clock arrangement process. Consequences of its SPICE reproduction, that identify with 1.2 lm CMOS innovation, demonstrated that the obligation cycle of the multistage yield heartbeats can be accurately changed in accordance with (50 ± 1)% inside the working recurrence run, from 55 MHz up to 166 MHz.

B.Nikolic, V.G.Oklobdzija, V.Stojanovic, W. Jia, J.K.S.Chiu,and M. M.- T.Leung, Improved sense-enhancer based flip-flounder designand measurements.Design and exploratory assessment of another senseamplifier-based flip-tumble (SAFF) is displayed. It was discovered that the fundamental speed bottleneck of existing SAFF's is the cross-coupled set-reset (SR) hook in the yield organize. The new flip-tumble utilizes another yield arrange hook topology that fundamentally decreases delay and enhances driving capacity. The execution of this flip-flounder is checked by estimations on a test chip actualized in 0.18 m compelling channel length CMOS. Shown speed places it among the speediest flip-flops utilized as a part of the cutting edge processors. Estimation systems utilized in this work and in addition the estimation set-up are talked about.

V.Stojanovic and V.G.Oklobdzija Comparative examination of ace slave locks and flip-flops for elite and low-control frameworks .We propose an arrangement of principles for predictable estimation of the genuine execution and power highlights of the flip-flounder and master– slave hook structures. Another reenactment and enhancement approach is introduced, focusing on both high performance

3. EXISTING SYSTEM

As transmission doors, is like a transfer that can direct in the two headings or square by a control motion with any voltage potential. n guideline, a transmission entryway made up of two field impact transistors, in which

rather than customary discrete field impact transistors - the substrate terminal (Bulk) is associated inside to the source terminal. The two transistors, a n-channel MOSFET and a p-direct MOSFET are associated in parallel with this, be that as it may, just the deplete and source terminals of the two transistors are associated together. Their door terminals are associated with each other by means of a NOT entryway (inverter), to frame the control terminal.

One of the exchanging terminals of the transmission door is raised to a voltage close to the negative supply voltage, a positive entryway source voltage (door to-deplete voltage) will happen at the N-channel MOSFET, and the transistor starts to direct, and the transmission entryway conducts. The voltage at one of the exchanging terminals of the transmission door is currently raised persistently up to the positive supply voltage potential, so the entryway source voltage is lessened (entryway deplete voltage) on the n-channel MOSFET, and this starts to kill. In the meantime, the p-channel MOSFET has a negative door source voltage (entryway to-deplete voltage) develops, whereby this transistor begins to lead and the transmission door switches.

Subsequently it is accomplished that the transmission entryway disregards the whole voltage go. The change protection of the transmission door fluctuates relying on the voltage to be switched,and relates to a superposition of the protection bends ofthe two transistors.

The control input ST must be able to take to control depending on the supply voltage and switching voltage different logic levels.To provide a basis for comparison, some existing FF designs are reviewed first. A classic master–slave-type TGFF design is shown in Fig. 1

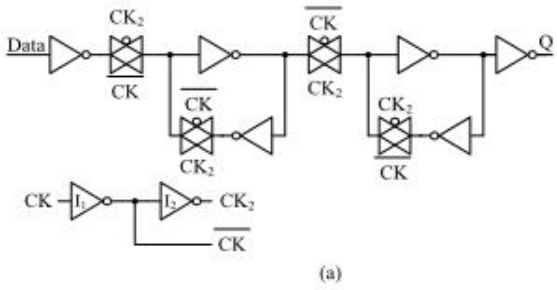

Fig1 Master Slave type TGFF

Indicating that it comprises two TG-based latch designs. Inverters I1 and I2 are used to generate complementary clock signals. This design suffers from a high capacitive clock loading problem (a total of 12 transistors driven by the clock), which indicates a sustained power consumption even when the input remains static . This problem also

occurs in conventional SRFF designs, as shown in Fig.1

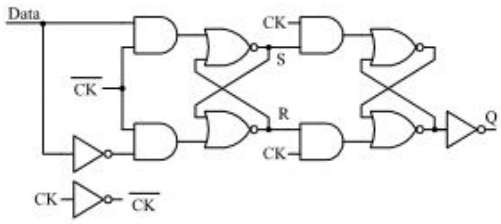

Fig4.3 Conventional SRFF designs

To overcome the power consumption problem, two FF designs employing an adaptive coupling (ac) technique and a topologically compressed scheme have been proposed. Fig. 3.7 shows the ac FF design .

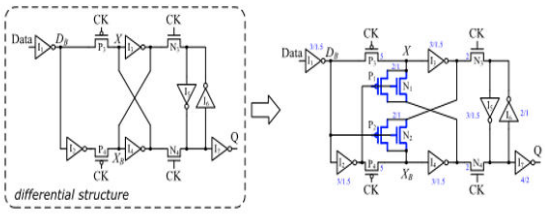

Fig2 AC Flipflop design

conventional TGFF designs, this design uses a differential latch structure with pass-transistor logic to achieve TSPC operation. The TGs are replaced with either n- or p-type pass transistors. To overcome the impact of process variations on the master latch, a pair of level restoring circuits is inserted into the crosscoupled paths of the master latch. In this design, only four MOS transistors (two pMOS and two nMOS) are driven by the clock signal, and the transistor countis lowered to 22. A lighter clock loading in addition to the circuit simplification of the FF design can lower the power consumption significantly. In this design, the data contention problem in the slave latch deteriorates as the data switching activity increases, and the advantages of power saving are thus diminished. The level restoring circuit pair of the master latch results in a longer setup time. Moreover, this design suffers from a power leaking problem when certain input and internal node combinations occur.

4. PROPOSED SYSTEM

In the proposed system design the transistor count is further reduced from 19 to 18. This reduction simplifies the circuit and the power consumption also reduced. Figure 3 shows the structure of 18 transistor FF design. In this design the transistor in the master latch is combined with the clock signal and thus the transistor count is reduced by one. The operation involves that when data=0 and clock is low the master latch becomes transparent and stores the data input. When data=1 and clock is high the master is in hold state and the slave latch changes its value that is the data stored in the master is transferred to slave and it is outputted to Q.The clock controlled NMOS transistor is also connected with the x2

discharging node. Hence, the power gets reduced and the delay also compromised. The set up time , hold time are in seconds.

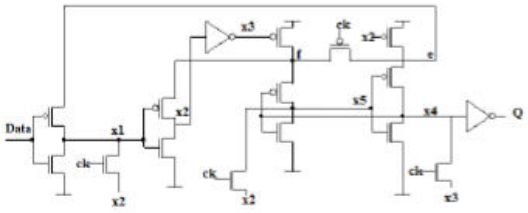

Figure 11: Proposed Flip-Flop design Both PDPCQ and PDPDQ were employed as a composite performance index in our evaluation. When the switching activity was 12.5%, both PDP indices of the proposed design were the lowest, followed by those of the TCFF and ACFF. However, the indices of the remaining four non-TSPC designs trailed by a large margin. The proposed LRFF design, in particular, can simultaneously balance the power and speed performance for the best results. Illustrates a bar chart summarizing the PDP comparison results under different switching activities. shows the PDP performance under process variations with a 25% data switching probability. For each process corner (SS 0.8 V/ 125 °C, TT 1 V/25 °C, FF 1.2 V/−40 °C, SF 1 V/25 °C, and FS 1 V/25 °C), the setup time and hold time were scanned to obtain the best PDP number. All FF designs were determined to function properly under process variations. Our design maintained its lead in all cases. Therefore, this evaluation also verifies the performance consistency of the LRFF design.

As indicated in the MOS schematic shown in Fig. 3.8 theconverged discharging path controlled by *x*2/*x*3 and CK in the slave latch is first split into two separate discharging paths, each comprising two nMOS transistors in series and implementingthe logic *x*2·CK·0 and *x*3·CK·0. If *x*2 = 1 (or *x*3 = 1*)*,it is logically equivalent to ¯ *x*2 ·CK (or ¯*x*3 ·CK*)*. Because *x*2 and *x*3 are complementary, ¯ *x*2 ·CK = *x*3 ·CK (or ¯ *x*3 ·CK = *x*2 ·CK*)*. As indicated in the small figure in Fig. 3.14 this term can be implemented using one pass transistor with CK as the control signal and *x*3 (or *x*2*)* as the sink of the discharging current.

The converged discharging path in the TCFF design can be split into two separate paths, each comprising one pass transistor. Because these two pass transistors operate in a complementary manner, they are considered as CPL, and the transistor count can thus be reduced by one. The benefit of this logic structure reduction is twofold. First, it simplifies the circuit for power saving. Although the pulldown delay might be slightly prolonged, it does not correspond to the worstcasetiming (in contrast to the

pull-up delay). Second, when node *x*2 (or *x*3*)* is equal to 1, the pass transistorworks in conjunction with the pull-up path formed by pMOS transistors *p*3/*p*4 (or *p*5/*p*6*)* to boost the output node of AOI to 1. This path is considered auxiliary because a "weak 1" can be delivered by an nMOS pass transistor. This additionalcurrent boost, however, improves the worst case delay when the slave latch is in the transparent mode (CK = 1). A shorter clock-to-Q (CQ) delay can be obtained. The dotted and solid arrowed lines in Fig. 3.14 indicate the working of these two charging paths to drive node *x*5 (or *x*4*)*. The second logic structure reduction scheme is applied to the second AOI gate of the master latch. The discharging path of node *x*2 controlled by CK and *x*3 discharges only when both signals equal 1. As illustrated in Fig. 3.18 pass transistor *n*7in addition to pull-down transistor *n*8 controlled by *x*4 forms an alternative discharging path for node *x*2. We can thus remove the original (and redundant) path to simplify the circuit. This measure not only improves the power performance but also reduces the capacitive load of node *x*2. A shorter propagation delay can be achieved for the master latch when operating in the transparent mode, resulting in a shorter setup time of the FF design. The circuit schematic after the application of the two logicstructure reduction schemes is presented in Fig. 3.19. The total number of transistors is only 19. Only one single phase of the clock is required, and the fan-out for the clock signal is four (one pMOS and three nMOS transistors). The proposed LRFF is fully static and can avoid the case of temporary output node floating. When CPL is introduced, the circuit complexity of its p-logic network is largely reduced, even though the design is not a dynamic logic. In conclusion, the proposed design can successfully achieve circuit complexity reduction and timing parameter enhancement simultaneously.

7.1 RESULT

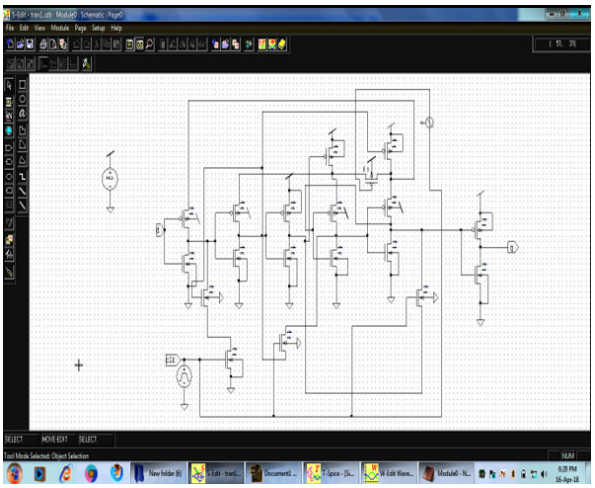

Fig7.1 Circuit connection of Master- slave D-flip-flop using TCFF technique

CONCLUSIN AND FUTURE SCOPE

We present a novel FF design achieved by employing a modified SR latch structure

incorporating a hybrid logic consisting of static-CMOS logic and CPL. The key idea is providing an additional discharge path between the master and slave latches, which not only shortens the transition time to enhance the power and speed performance, but also reduces circuit complexity for better timing parameters. Extensive simulations were conducted and various performance indices such as power consumption, PDP, setup time delay, and CQ delays were evaluated. The proposed design was determined to excel in almost every performance index, except for hold time performance. In particular, the proposed design consistently outperformed other designs under different voltage and switching activity settings. This thus proves the efficiency of the proposed FF design.We hope that presented results will encourage further research activities in TCFF technique. The issue of sequential logic design with TCFF is currently being explored, as well as technology compatibility. More work was recently done in automation of logic design methodology based on TCFF technology.

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